Hardware Topics

Russell

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Agenda

- Interface
  - Local bus
    - ISA
    - PCI
  - USB
  - MII
  - GMII
  - UTP

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Agenda (cont.)

- Davicom products
  - PHY
  - NIC
  - Switch
- EMC
  - ESD
  - EMI

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Local Bus

Interface

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ISA Local bus

- Concept
  - Control bus group
  - Address bus group
  - Data bus group
- Bus speed
  - 50M x bus width (burst read/write)

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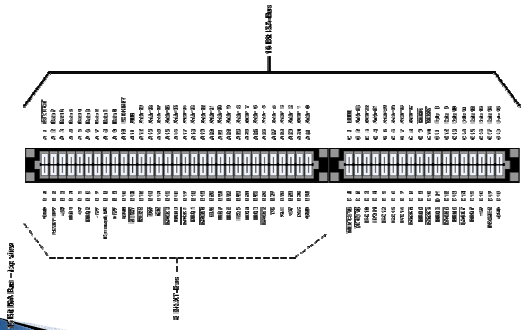
ISA Local bus (cont.)



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PCI Local Bus

- Benefit
  - High speed – 1056Mbps peak
  - Low latency random access – 60ns

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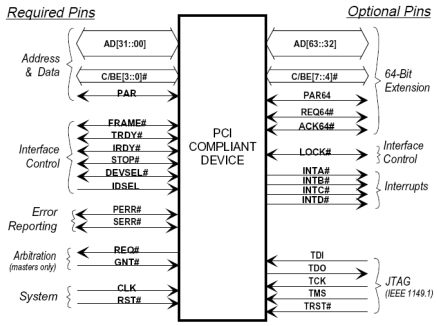
PCI Local Bus (cont.)



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Universal Serial Bus (USB)

» Interface

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USB

- Taxonomy
  - 1.0/1.1 – 12Mbps
  - 2.0 – 480Mbps

Performance	Application
Low Speed 10-100kbps	Keyboard, mouse, etc.
Full Speed 500kbps-10Mbps	Broadband, Audio, etc.
High Speed 25-400Mbps	Video, Storage, Broadband, etc.

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USB (cont.)

- System description
  - USB interconnect
  - USB devices
  - USB host

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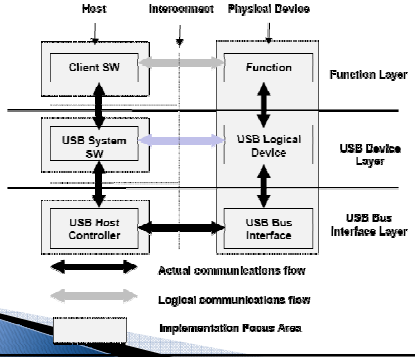
USB (cont.)

- Implementation area



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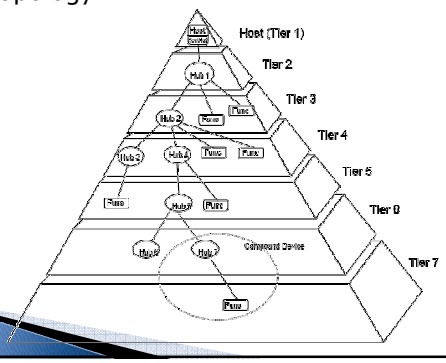
USB (cont.)

- Bus topology



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Media Independent Interface (MII)

- Interface

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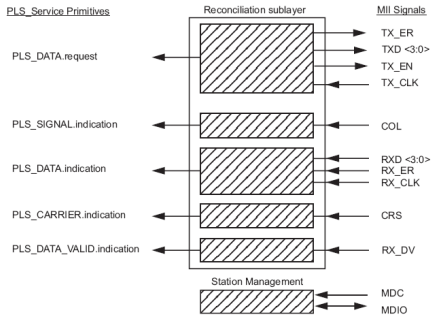
MII



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MII (cont.)

- Conductor size:
  - 0.32mm (AWG 28)
- Characteristic Impedance:
  - 68 ohm ± 10%
- Delay:
  - 2.5ns
- Delay variation:
  - 0.1ns

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RMII

MII	RMII
TXD[1:0]	TXD[1:0]
TXD[3:2]	
TXEN	TXEN
TXER	
TXCLK	
RXD[1:0]	RXD[1:0]
RXD[3:2]	
RXER	RPTR
RXDV	CRS DV
RXCLK	
COL	
CRS	
25MHz	50MHz

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Gigabit Media Independent Interface (GMII)

- Interface

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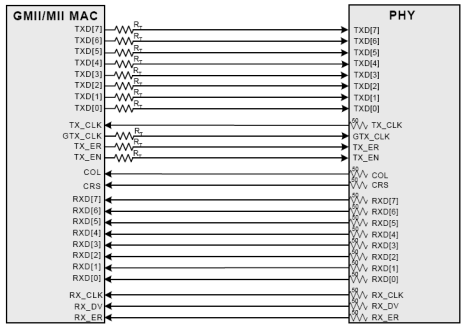
GMII



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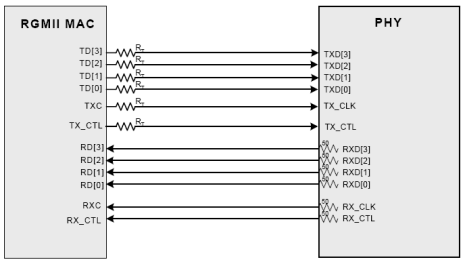
RGMII



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Unshielded Twisted Pair (UTP)

- Interface

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UTP

- 10/100 UTP assignment

Contact	Without cross over MDI	With cross over MDI (MDI-X)
1	Transmit +	Receive +
2	Transmit -	Receive -
3	Receive +	Transmit +
4		
5		
6	Receive -	Transmit -
7		
8		

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UTP

- 1000 UTP assignment

Contact	Without cross over MDI	With cross over MDI (MDI-X)
1	D1 +	D2+
2	D1 -	D2-
3	D2 +	D1 +
4	D3+	D4+
5	D3-	D4-
6	D2 -	D1-
7	D4+	D3+
8	D4-	D3-

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UTP

- Differential Characteristic Impedance:
  - 100 ohm
- Insertion Loss
  - $IL(f) < 2.1f^{0.529} + \frac{0.4}{f}$
- Return Loss
  - $RL(f) = \begin{cases} 15 & (1-20MHz) \\ 15-10\log(\frac{f}{20}) & (20-100MHz) \end{cases}$
- Differential Near-End Cross Talk
  - $NEXT = 27.1-16.8\log(\frac{f}{100})$

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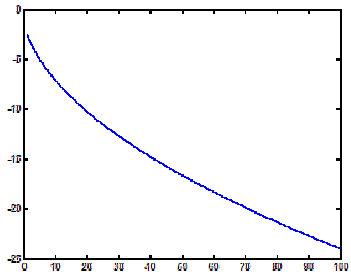
UTP – Insertion Loss



$$IL(f) < 2.1f^{0.529} + \frac{0.4}{f}$$

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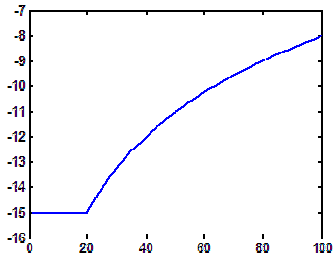
UTP – Return Loss



$$RL(f) = \begin{cases} 15 & (1-20MHz) \\ 15-10\log(\frac{f}{20}) & (20-100MHz) \end{cases}$$

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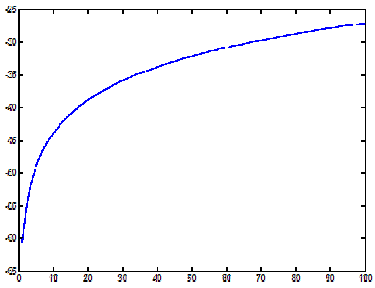
UTP – NEXT



$$NEXT = 27.1 - 16.8\log(\frac{f}{100})$$

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UTP (cont.)

- Transformer Return Loss
Frequency	Value
30MHz	-26dB-ohm
159MHz	-13dB-ohm
500MHz	-5dB-ohm

Go back Page 49

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Differential Line

- Benefit
  - Increase the immunity of noise
  - High speed
  - Decrease the EMI

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Differential Line (cont.)

- Single Line

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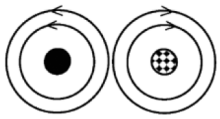
Differential Line (cont.)

- Differential Line



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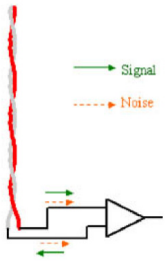
Differential Line (cont.)



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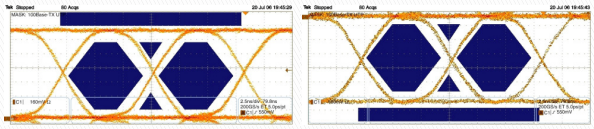
IEEE 802.3 test



Positive Amplitude | Negative Amplitude

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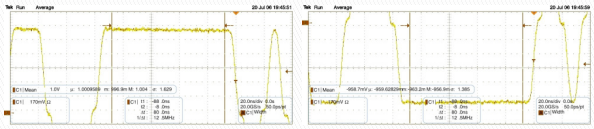
IEEE 802.3 test (cont.)



Positive Amplitude | Negative Amplitude

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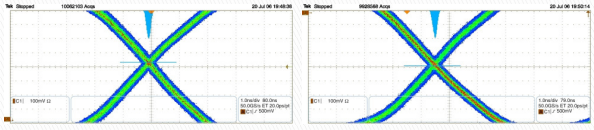
IEEE 802.3 test (cont.)



Positive Amplitude | Negative Amplitude

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PHY

- Davicom products

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PHY

- DM9161
- DM9161A
- DM9161B
- DM9161BI

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DM9161 series comparison

- Main difference between DM9161E, DM9161AE and DM9161BE

Item	DM9161	DM9161A	DM9161B
Process	.35μm	.25μm	.18μm
PHY Type	Analog	Analog	DSP

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DM9161 series comparison (cont.)

- Function difference between DM9161E, DM9161AE and DM9161BE

Function	DM9161	DM9161A	DM9161B
Auto-MDIX	No	Yes	Yes
Power Saving Mode for 10Base-T	No	No	Yes

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DM9161 series comparison (cont.)

- Power difference between DM9161E, DM9161AE and DM9161BE

Item	DM9161	DM9161A	DM9161B
Power	3.3V	3.3V	3.3V
Built-in Regulator	No	Yes/2.5V	Yes/1.8V

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DM9161 series Power Consumption Comparison

Item	DM9161E	DM9161A	DM9161B	SMSC LAN8187	SMSC LAN8700	Realtek RTL8201DL
Pin counts	48	48	48	64	36	48
PHY Type	Analog	Analog	DSP	DSP	DSP	DSP
Power Consumption (mW)						
100Base-TX	290.4	303.6	429	246.84	246.84	346.5
10Base-T	231 (50%)	237.6 (50%)	554.4	122.1	122.1	429
10Base-T (power saving)	NA	NA	201.3	83.88	83.88	NA
10Base-T idle	99	82.5	NA	NA	NA	82.5
Auto-Negotiation	148.5	171.6	191.4	NA	NA	NA
Power Reduced Mode (without cable)	59.4	82.5	NA	NA	NA	NA
Power Down Mode (system clock off)	9.9	12.54	56.1	10.13	10.131	56.1

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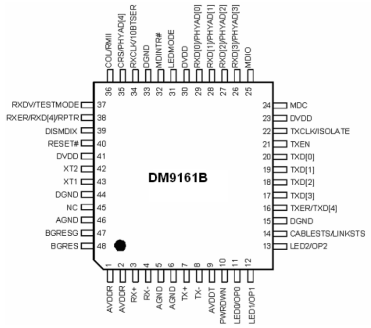
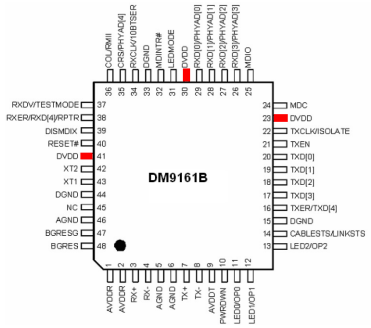
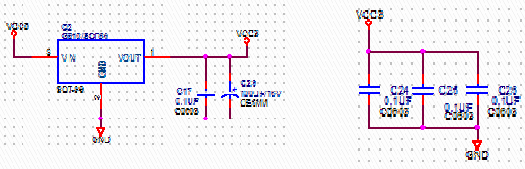
DM9161 series IC view



Schematic- Power



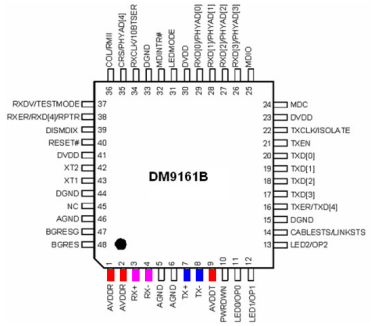
Schematic – Power (cont.)



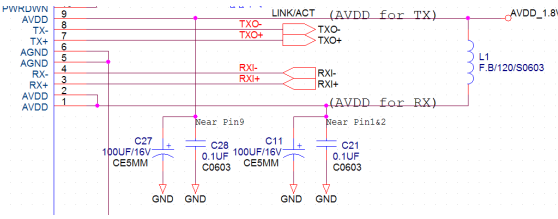
5V to 3.3V Regulator

Decoupling Capacitors

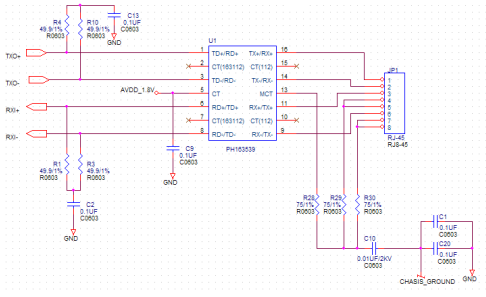
Schematic- Differential Lines



Schematic- Differential Lines (cont.)

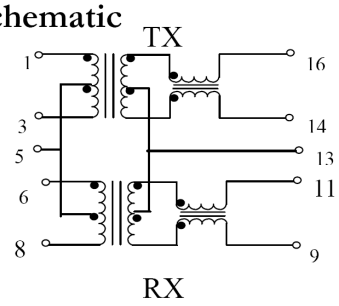


Schematic- Differential Lines (cont.)



Transformer

Schematic



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Transformer (cont.)

Specifications										
Part Number	Turn Ratio		Insertion Loss 0.3~100MHz (dB MAX)	Return Loss (MHz)			CMRR (dB)			Hi-Pot (Vrms MIN)
	Tx	Rx		30MHz	60MHz	100MHz	30MHz	50MHz	100MHz	
HS9016	1:1	1:1	1.0	-18 dB	-16dB	-12dB	-45db	-40dB	-35dB	1500
LF-HS9016	1:1	1:1	1.0	-18 dB	-16dB	-12dB	-45db	-40dB	-35dB	1500

Refer to Page 28

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Transformer (cont.)

Specifications										
Part Number	Turn Ratio		Insertion Loss 0.1~100MHz (dB MAX)	Return Loss (MHz)			CMRR (dB)			Hi-Pot (Vrms MIN)
	Tx	Rx		30MHz	60MHz	80MHz	30MHz	50MHz	100MHz	
HS9001	1:1	1:1	1.1	-20db	-14dB	-11.5dB	-42db	-37dB	-33dB	1500
HS9002	1.414:1	1:1	1.1	-20db	-14dB	-11.5dB	-42db	-37dB	-33dB	1500
HS9003	1.25:1	1:1	1.1	-20db	-14dB	-11.5dB	-42db	-37dB	-33dB	1500
HS9004	2:1	1:1	1.1	-20db	-14dB	-11.5dB	-42db	-37dB	-33dB	1500
HS9005	1:1.414	1:1	1.1	-20db	-14dB	-11.5dB	-42db	-37dB	-33dB	1500
HS9006	1:1.25	1:1	1.1	-20db	-14dB	-11.5dB	-42db	-37dB	-33dB	1500

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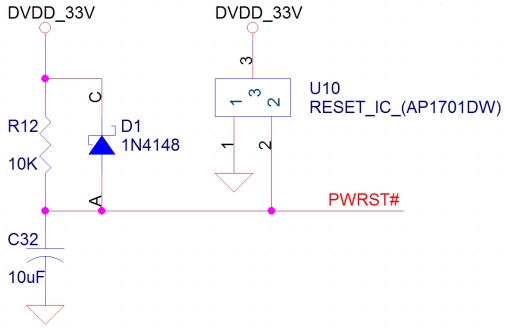
Schematic – Reset#



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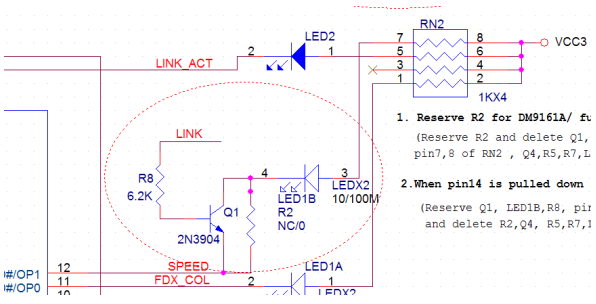
Schematic– LEDs



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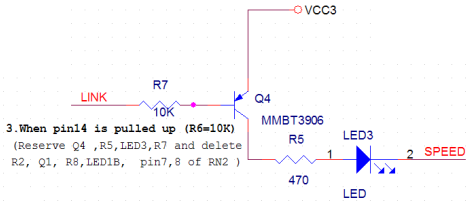
Schematic – LEDs (cont.)



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Easy way to debug itself – External Loopback

- Use external loopback
  - Short pin 1 and 3 and pin 2 and 6 of cable.
- Transmit broadcast packets
- Verify receive packets

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NIC

Davicom products

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NIC

- ISA – Local bus
- PCI – Local bus
- USB

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NIC – ISA – Local Bus

Davicom products

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ISA Local bus product

- 8/16 bits
  - DM9000A
  - DM9000B
  - DM9000BI
- 8/16/32 bits/MII
  - DM9000
  - DM9010
  - DM9010B

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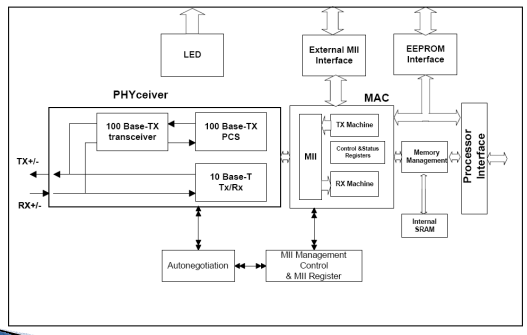
Block Diagram



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Features

- 10/100 with Auto MDIX
- Flow control
- Back pressure
- 16K Bytes internal SRAM

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The Difference of DM9000A series

Item	DM9000A	DM9000B
Production Process	0.25um	0.18um
PHY type	Analog	DSP
Output voltage of built-in regulator	2.5V	1.8V
Power saving mode for auto-negotiation	No	Yes

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The Difference of DM9000 series

Item	DM9000	DM9010	DM9010B
Production Process	0.35um	0.25um	0.18um
PHY Type	Analog	Analog	DSP
Built-in Regulator	None	2.5V	1.8V
Power saving mode for auto-negotiation	No	No	Yes
TX engine	1	2	2

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DM9000 series Power Consumption Comparison

Item	DM9000	DM9000A	DM9000B	SMSC LAN9211	SMSC LAN9115	Asix AX88796B
Pin counts	100	48	48	56	100	64
PHY Type	Analog	Analog	DSP	DSP	NA	NA
Power Consumption (mW)						
100Base-TX	330	287.1	429	514	422	495
10Base-T	280.5	303.6	561	578	244	462
10Base-T (power saving)	NA	NA	528	NA	120	NA
10Base-T Idle	145.2	125.4	198 (power saving)	569	225	448 (power saving)
Auto-Negotiation	198	184.8	198	NA	NA	587
Power Reduce Mode	66	102.3	NA	NA	NA	NA
Power Down Mode	NA	69.3	NA	61	35	140
Power Down Mode (system clock off)	33	23.1	66	10	11	0.9 (D2)

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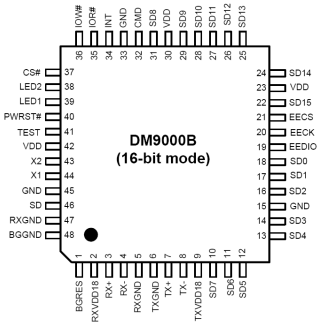
DM9000A/DM9000B - 16-bit



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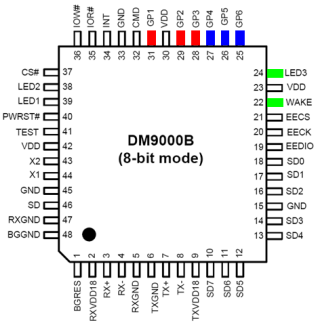
DM9000A/DM9000B – 8-bit



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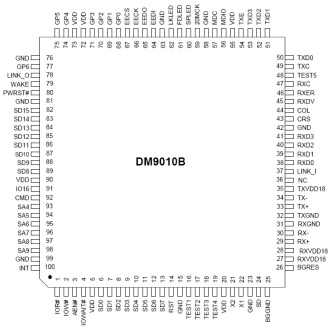
DM9000/DM9010/DM9010B – MII



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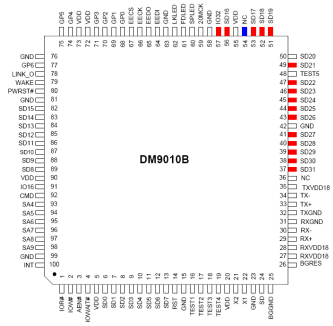
DM9000/DM9010/ DM9010B – 32-bit



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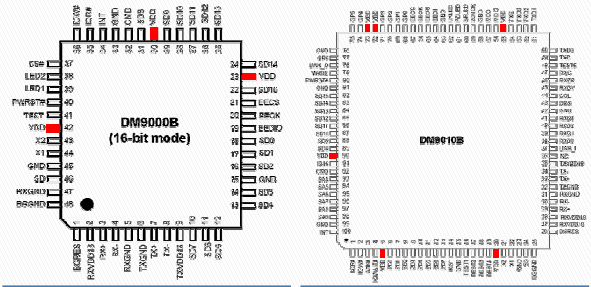
Application Schematic – Power



DM9000B | DM9010B

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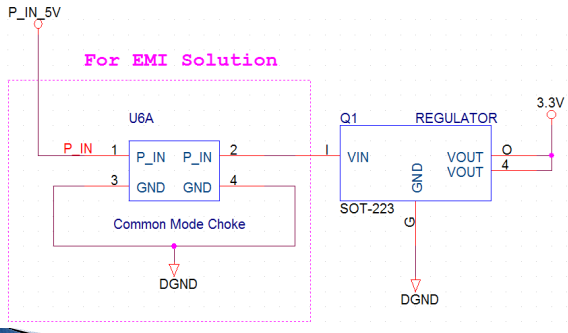
Application Schematic – Power (cont.)



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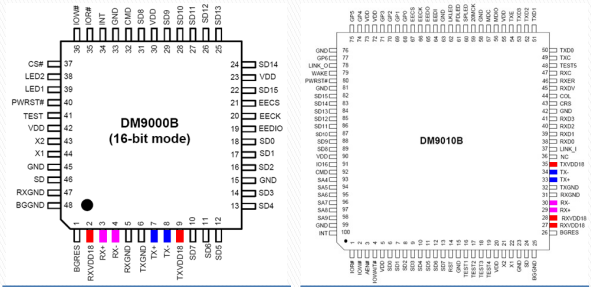
Application Schematic – RJ-45



DM9000B | DM9010B

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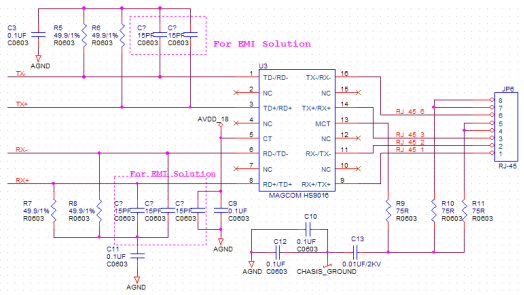
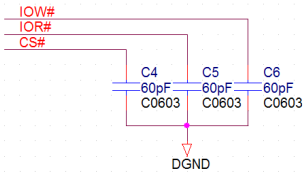
Application Schematic – RJ-45 (cont.)



Application Schematic – Data Bus



Decoupling Capacitors

Easy way to debug itself – PHY Internal Loopback

- Power up PHY
  - MAC register 1FH bit 0 = 0
- Set up loop back mode
  - Write PHY register 00H bit 14 = 1
  - Write PHY register 10H bit 7 = 1
- RX enable
  - Write MAC register 05H bit 0 = 1
- Transmit broadcast packets
- Verify the receive packets

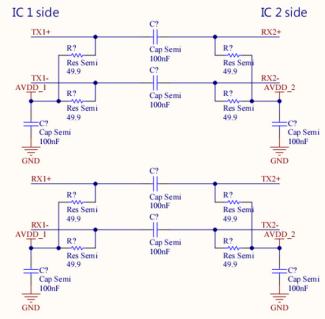
Easy way to debug itself – MAC Internal Loopback

- Enable MAC loopback
  - Write MAC register 00H bit 2:1 to 01
- Transmit broad cast packets
- Verify receive packets

Application Note

- DM9000B 1.8V becomes around 1.2V
  - Due to Auto-Negotiation Power Saving mode
  - Disable by writing PHY Register 20 bit 11 to 1.

Application Note (cont.)



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NIC – PCI – Local Bus

- Davicom products

80

PCI Local Bus Products

- DM9102A
- DM9102D
- DM9102H

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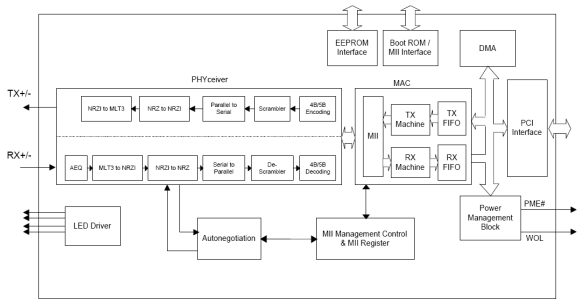
Block Diagram



82

Features

- 10/100 with Auto MDIX
- Flow control
- Back pressure

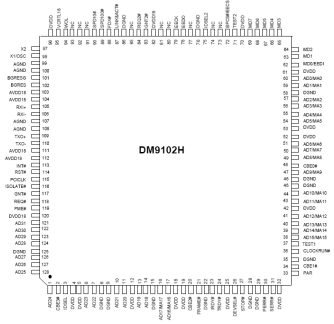
83

Difference between DM9102 series

Item	DM9102A	DM9102D	DM9102H
Process	0.35um	0.25um	0.18um
Package	QFP	LQFP	LQFP
PHY Type	Analog	Analog	DSP
Built-in Regulator	No	2.5V	1.8V
Power Saving Mode for Auto-Negotiation	No	No	Yes

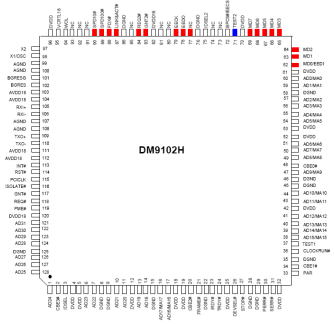
84

DM9102H normal mode



85

DM9102H with MII mode



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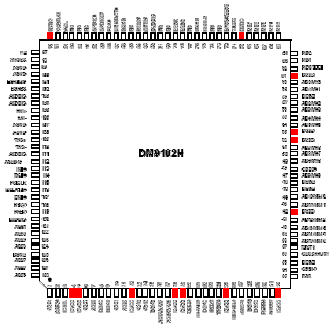
Application Schematic – Power



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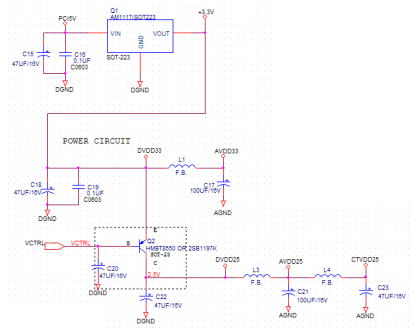
Application Schematic – Power



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NIC – USB

- Davicom Products

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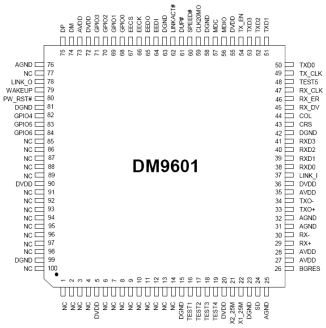
DM9601



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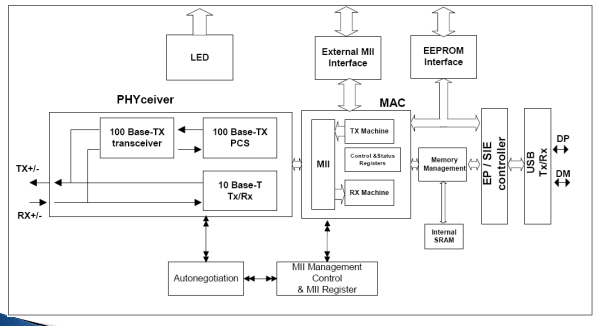
Block Diagram



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Features

- 16K bytes SRAM
- USB 1.1 device
  - up to 12Mbps
- Supports MII/Reverse-MII

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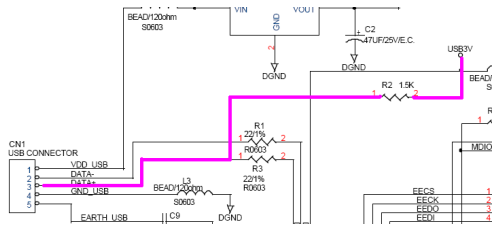
Schematic



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Switch

Davicom Products

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Switch

- Local bus
  - DM9003
  - DM9013
- PCI
  - DM9103
- Pure
  - DM8203

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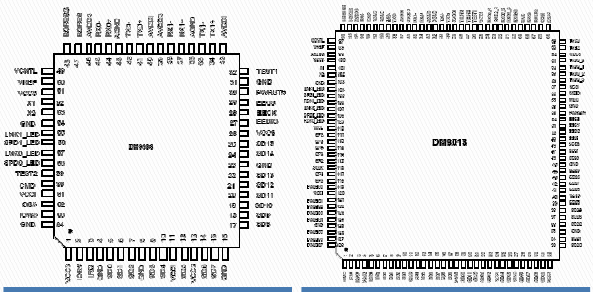
DM9003/DM9013



DM9003 | DM9013

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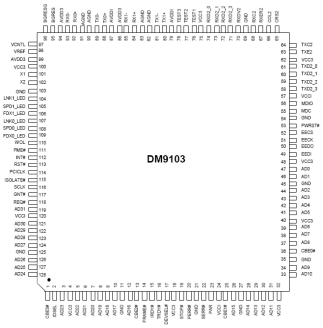
DM9103



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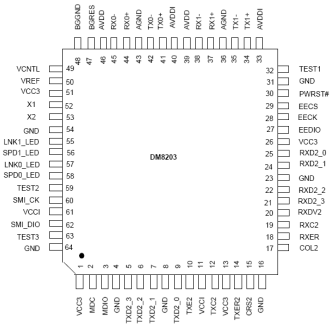
DM8203



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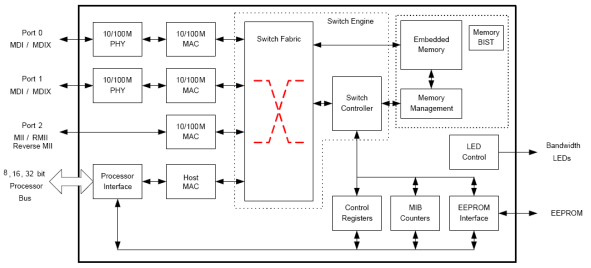
Block Diagram – DM9013



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Switch function

- 1K unicast MAC address learning
- Automatic aging
- Broadcast storming filter
- MIB counter for debug
- Bandwidth egress/ingress control
- Support 16 VLAN groups
- VLAN ID tag/untag
- Priority control
  - Port based
  - 802.1p VLAN
  - IP ToS

102

Future functions for DM9016

- IGMP
- MLD
- Span tree

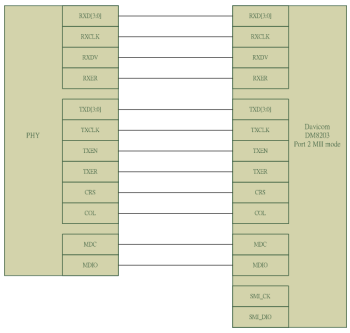
103

Difference of ICs

Item	DM8203	DM9003	DM9013	DM9103
Pin count	64	64	128	128
Port count	2 PHYs	2 PHYs	2 PHYs + 1 MAC	2 PHYs + 1 MAC
Processor port	MII	ISA local bus	ISA local bus	PCI local bus
Data bus width	4	8/16	8/16/32	32
Industrial Temperature Level	No	Yes	Yes	No

104

DM8203 MII mode connection



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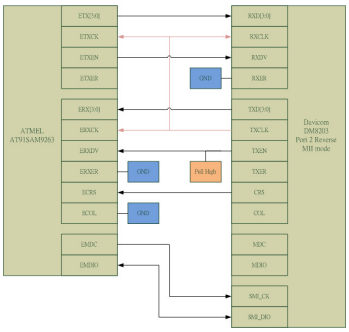
DM8203 Reverse-MII mode connection



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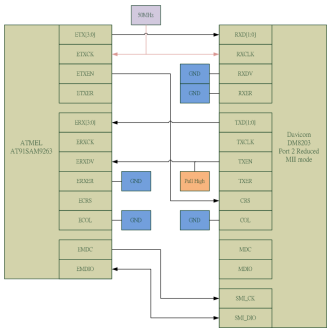
DM8203 Reduced-MII mode connection



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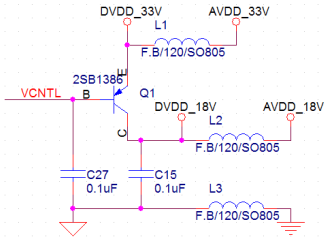
Schematic – 1.8V Voltage Control



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Application Note

- Metanoia PHY (VDSL convertor)
  - For DM8203/DM9013/DM9103
  - The preamble can't be reduced

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Heat problem

- Working out!

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ESD

EMC

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Component ESD

- DM9161B
  - 7KV
- DM9000B/DM9010B
  - 5KV
- DM8203/DM9003/DM9013/DM9103
  - 7.5KV

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System level ESD Standard

- Contact
  - 4KV
  - 15 times
- Air
  - 8KV
  - Around the DUT

Commercial

- Contact
  - 8KV
  - 15 times
- Air
  - 16KV
  - Around the DUT

Industrial

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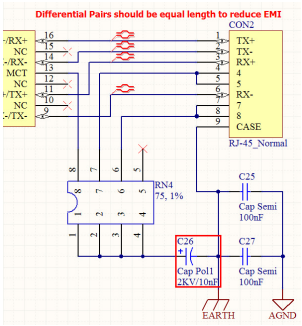
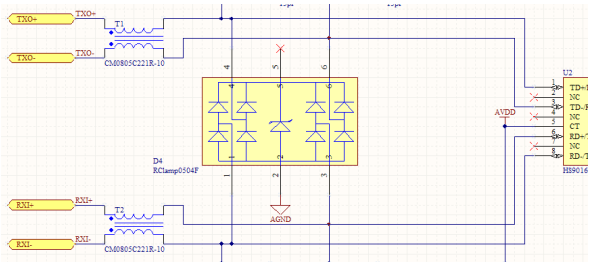
Hi-Vol Capacitor



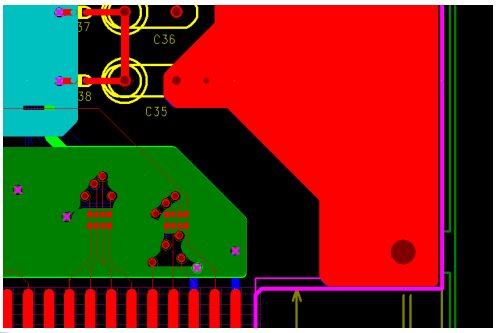
TVS



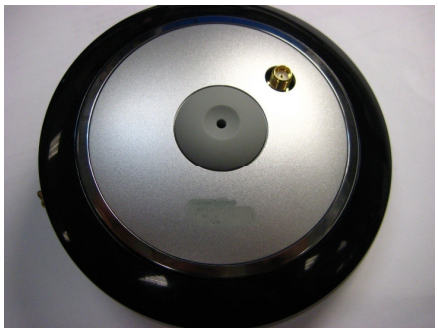
Layout technique

- Gap between Earth and Ground
  - 1mm for 2KV
- A low impedance way

Layout technique

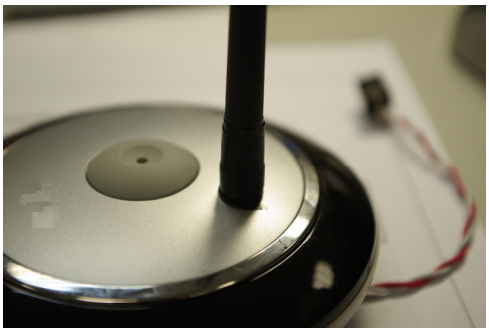


Case



Case (cont.)

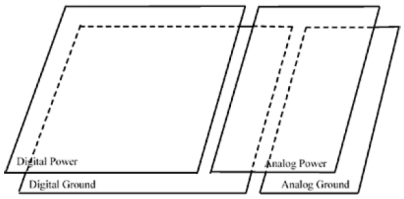
Case (cont.)



EMI

- EMC

Power Planes



Stack up

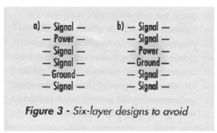


Figure 3 - Six-layer designs to avoid

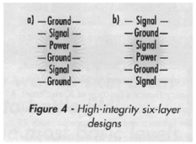


Figure 4 - High-integrity six-layer designs

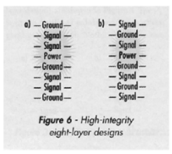


Figure 6 - High-integrity eight-layer designs

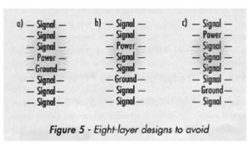
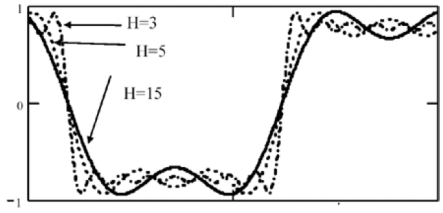


Figure 5 - Eight-layer designs to avoid

Signal Integrity – Square Wave

- Component



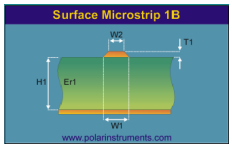
$$Square(\theta) = Cos(\theta) - \frac{Cos(3\theta)}{3} + \frac{Cos(5\theta)}{5} - \frac{Cos(7\theta)}{7} + etc$$

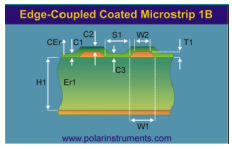
Signal Integrity – Square Wave (cont.)

- Square Wave Demo Program

Transmission Line

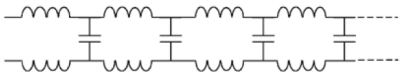
- The signal path to propagate the signal without loss or lossless.
- Several models for different purpose.





Signal Integrity – Impedance Match

- Transmission Line Model



- Characteristic Impedance

$$Zo = \sqrt{L/C}$$

- Reflection coefficient

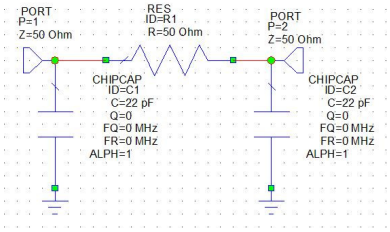
$$\rho = \frac{RL - Zo}{RL + Zo}$$

Signal Integrity – Impedance Match (cont.)

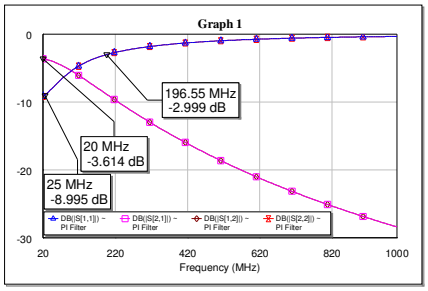
- Impedance Match Demo Program

Signal Integrity – real case

Signal Integrity – real case (cont.)



Signal Integrity – real case (cont.)



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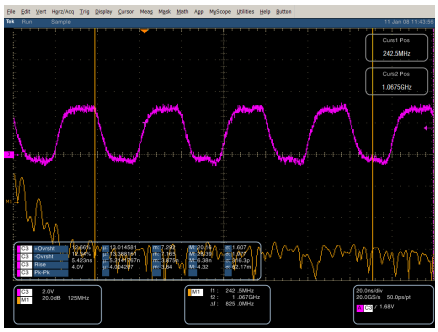
Signal Integrity – real case (cont.)



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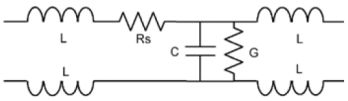
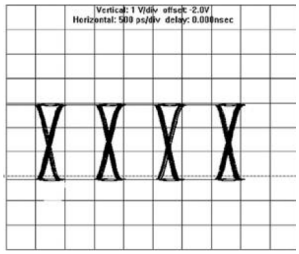
Lossy Line



$$Zo = \sqrt{\frac{Rs + j\omega L}{G + j\omega C}}$$

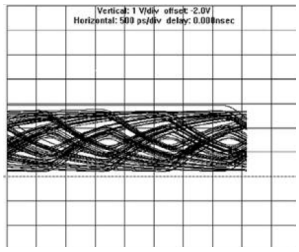
135

Lossy Line (cont.)



136

Lossy Line (cont.)



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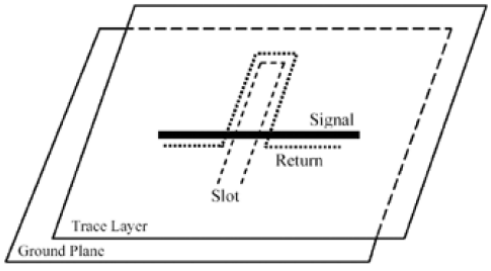
Return Current



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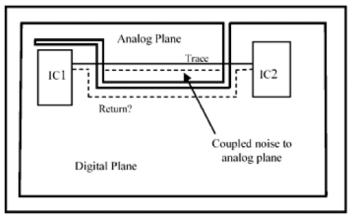
Return Current (cont.)



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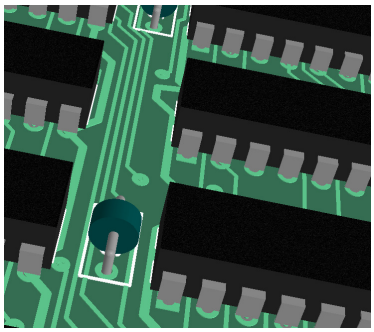
VIA



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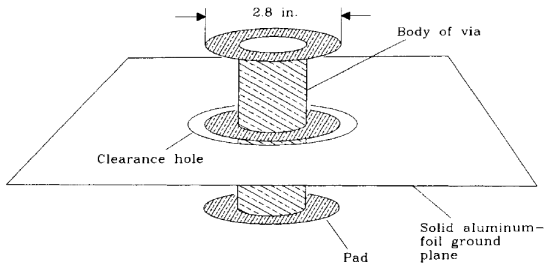
VIA (cont.)



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VIA (cont.)

- Increase the capacitance and inductance on the signal trace.
- Induce the EMI on intermediary layers.

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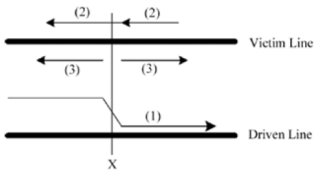
Parallel signal trace

- Crosstalk
  - Destroy the signal integrity
  - Increase the EMI
- How it happen



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Parallel signal trace (cont.)

- How to avoid
  - Place traces in stripline environments.
  - Minimize the distance between the trace and the plane.
  - Maximize the separation between the traces.
  - Consider the beneficial effects of near-end terminations.

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Parallel signal trace (cont.)

- Crosstalk Demo Program

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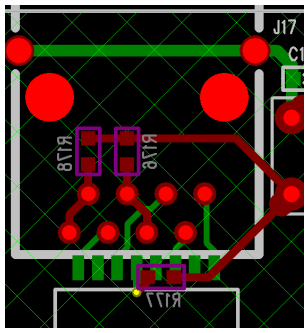
Crossover of signal trace



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Thank You!

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