Designing embedded Ethernet devices

By

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Inhalt

1   Introduction

The provided information shall support the designer when developing products with DAVICOM's Ethernet products. Although we can offer additional assistance to our customers in the design-in phase we cannot guarantee the performance of the finished design nor can we assume responsibility for the operation, in production.

Nowadays, in embedded systems, there is a strong urge to be able to control these systems via a network-connection by means of a browser or similar tools. Therefore a lot of modern microcontrollers come with an integrated Ethernet MAC or can easily be attached to an external MACPHY.

As external PHY or MACPHY a variety of components is on the market. Davicom with its PHYs and MACPHYs, is one of the market leaders. Although Davicom offers other Ethernet products like switches, USB-to-Ethernet converters and Copper-to-Fiber converters, this paper mainly deals with their PHYs and MACPHYs and concentrates on the physical layer and Media Independent interfaces.

While digital logic gets faster and faster, digital design has to deal with higher frequencies and that is where they become "analog" again. Having signal rise times of 1ns or even below implies that you have to deal with frequencies up to the GHz range if we can believe M. Fourier and his theorem. PCB design for circuits like that, means that you have to obey a lot of rules concerning high frequency design and compliance with the EMI regulations.

Also a deeper knowledge of the safety regulations for telecommunication equipment is mandatory as well as a good understanding of the Ethernet standards – mainly the IEEE 802.3. Also you should think about implementing testability in an early stage of the design phase. Test equipment for compliance testing of the physical layer and for the media access layer (layer 1 and 2 of the OSI model) has become less expensive.

Last but not least there are software decisions, like using an operating system on the MCU or preferring to use a bare-metal-system. In the latter case you are responsible for all the drivers yourself which can make your software engineer's life very miserable. To ease his pain check for off-the-shelf drivers for the processor of your choice. If you decided to go with an operating system that already implements the lower layers you carefully should estimate the performance.

But now let's start with the first chapter …

2   A look at the physical layer

2.1   Overview

Since this is only a short paper we will only concentrate on 10Mbit and 100Mbit trans-fer rate and a copper medium. In particular this is a twisted pair medium (10BASE-T) and (100BASE-TX) can be found in IEEE802.3 (2008).

For Fast Ethernet (100BASE-TX) in addition the Medium Dependent part (TP-PMD) is described in ANSI INCITS 263-1995 (S2010) with changes described in IEEE802.3 clause 25.3 and 25.4. All IEEE802.x standards are available for download on the IEEE homepage. ANSI standards can be ordered as PDF for the ANSI organisation's webstore (http://standards.ieee.org/about/get/ and http://webstore.ansi.org/).

In order to understand the physical layer for 10BASE-T have a look at clause 14.1.1 of IEEE802.3. It shows the relationship between the OSI reference model and the IEEE 802.3 CSMA/CD LAN model:
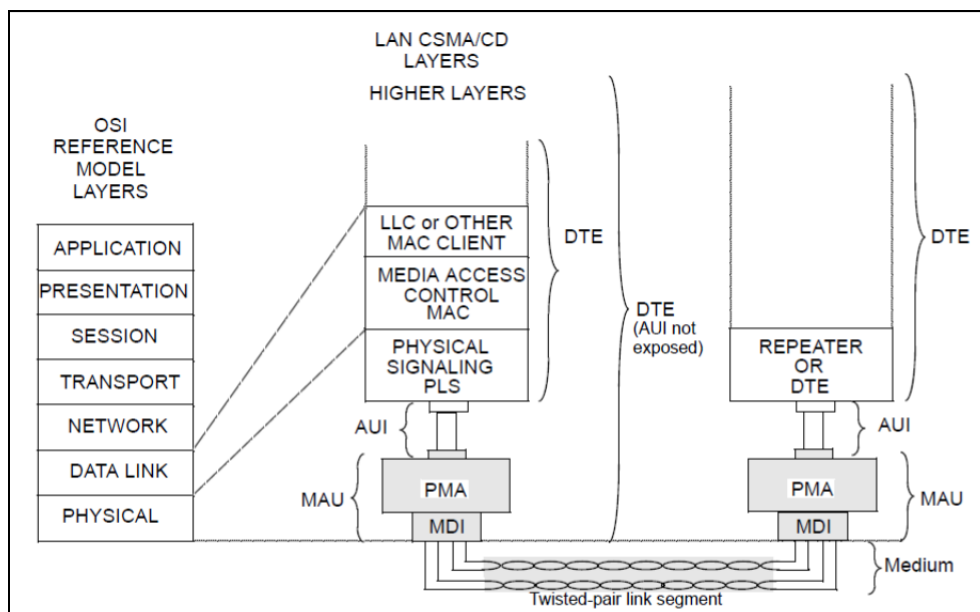

Figure 1: 10BASE-T relationship to the OSI reference model (taken from IEEE 802.3-2008)

The physical twisted pair connection (medium) attaches to the Media Dependent In-terface (MDI) which is part of the Media Access Unit (MAU) and is connected to the Physical Medium Attachment (PMA). This connects through the Attachment Unit In-terface (AUI) to the Physical Layer Signaling (PLS). All together form the physical layer (layer 1) of the OSI model. This layer now attaches to layer 2 (the Data Link layer) via an Media Independent Interface (MII, not shown here). The last sublayer in OSI layer 1 is the Reconcilation Sublayer (RS) followed by the Media Access Control (MAC), the first sublayer of OSI layer 2. This is visible in the more general illustration in Figure 2.
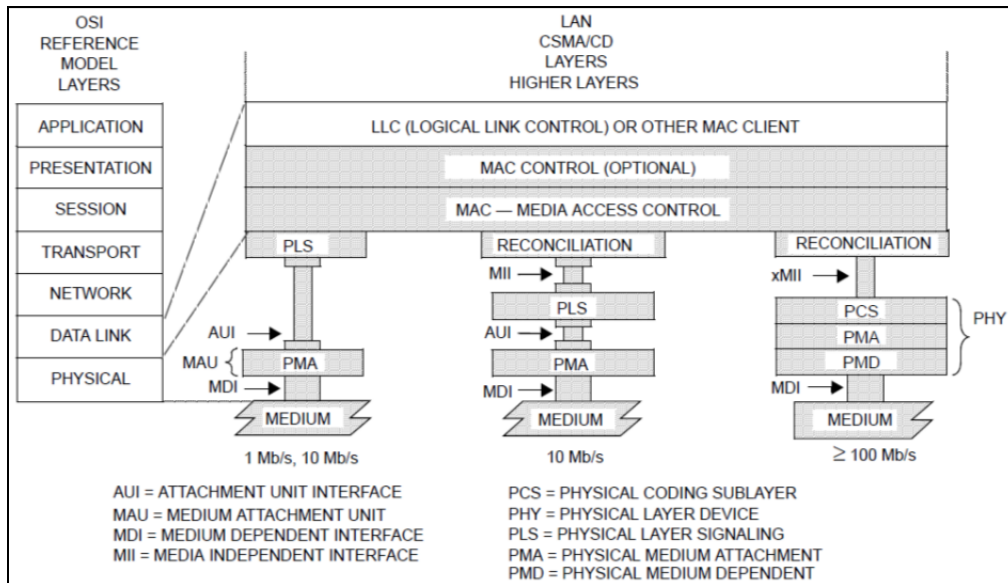
Figure 2: More general relationship to the OSI reference model (taken from IEEE 803.3-2008)

Generally what we call the "PHY" is a realization of the OSI physical layer with two interfaces: The Media Dependent Interface (MDI) and the Media Independent Interface (MII) which connects to the MAC of the processor. If the processor has no MAC we can use a MACPHY (a combination of the physical layer and parts of the data link layer (the driver that is realized on the processor also belongs to layer 2).

2.2   The Media Dependent Interface

2.2.1 Physical connection

The MDI uses the RJ45 connection made of an Modular 8/8 receptacle and an Modular 8/8 plug with a standardized pinning

Contact	MDI signal
1	TD+
2	TD-
3	RD+
4	Not used by 10BASE-T
5	Not used by 10BASE-T
6	RD-
7	Not used by 10BASE-T
8	Not used by 10BASE-T

Table 1: MDI connector for twisted pair link as shown in IEEE 803-3(2008) clause 14.5.1

There is also an MDI-X interface described where the MAU does an internal crossover for transmit and receive differential pair (which can be as simple as routing TD to RD and vica versa at the connector which then shall be marked with an X). If the PHY automatically detects the receive and transmit pair and does the crossover ac-

cordingly, this is called Auto-MDI-X. Most modern PHYs come with an Auto-MDI-X feature which can be switched on and off by Software.

2.2.2 Electrical safety

Although the Ethernet signal levels itself are SELV all network interfaces have a **safety requirement**! The general safety (refer to IEEC 802.3-2005 clause 14.7.1) shall meet IEC60950. The Network Safety (refer to IEEC 802.3-2005 clause 14.7.2) requires preventing from electrical hazard when touching a device that is connected via a network cable. Hazards that can appear are either direct contact of the LAN cable to power lines or any none safely extra-low voltage (SELV) circuits, static charge buildup on LAN cables, high energy transients due to for instance lightning and voltage potential differences between connected devices (see IEEE 802.3-2005 clause 14.7.2 a)-d). Safety grounding for such equipment and the impact of using a doubly insulated ac power supplies must be carefully considered and in compliance with IEC60950. The MAU to MDI interface requires an electrical isolation which can withstand at least one of the following tests (see IEC802.3-2005 clause 14.3.1.1):

- 1500V rms at 50Hz to 60Hz for 60s (see IEC60950-1:2005, 5.2.2)
- 2250V dc for 60s (see IEC60950-1:2005, 5.2.2)
- A sequence of ten 2400V impulses of alternating polarity, applied at intervals of not less than 1s (1.2/50us pulse as described in IEC6095-1:2005 Annex N)

There shall be no insulation breakdown and the resistance after the test shall be at least 500V dc (see IEC 60950-1:2005).

Please be aware that other requirements may be possible: If the device is a medical device, it must comply with IEC60601-1. For automotive design or aviation equipment there are other or additional requirements to meet which can depend on the customer as well.

The isolation requirement is the main reason why we need an Ethernet transformer and there should be no copper plane below the Ethernet magnetics and why this connection should be kept short (to meet a 1500V isolation requirement on a dense PCB which circuits are considered to be SELV is no fun!).
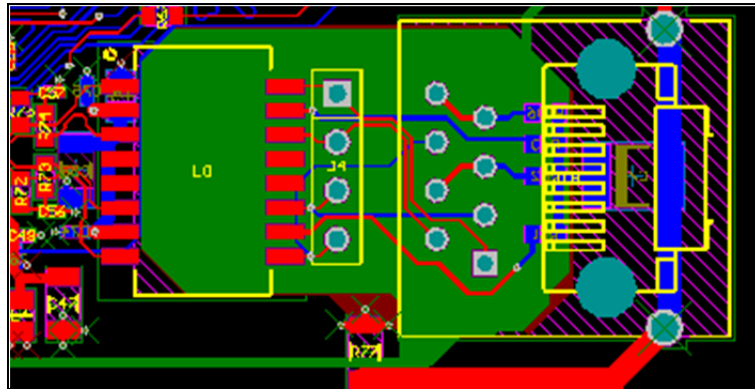
Figure 3: Layout example. The magnetics (L8) connect to the Modular receptacle.

Figure 3 shows an example of a layout. J4 is there to connect to a piggy back PCB with an alternative connection and yes – it causes an additional impedance "bump" and that's not nice! The PHY is connected to the magnetic's pads on the right side by means of a differential strip line. Since the connection is really short the connection is not that critical. This is a 4 layer PCB with a VCC and GND plane on layer 2 and 3. The green polygon is the cutout in the VCC and GND plane. The sole reason for the cutout is the isolation requirement! Since without the plane an impedance control of the connection between magnetics and connector is almost impossible and therefore this connection should be as short as possible.
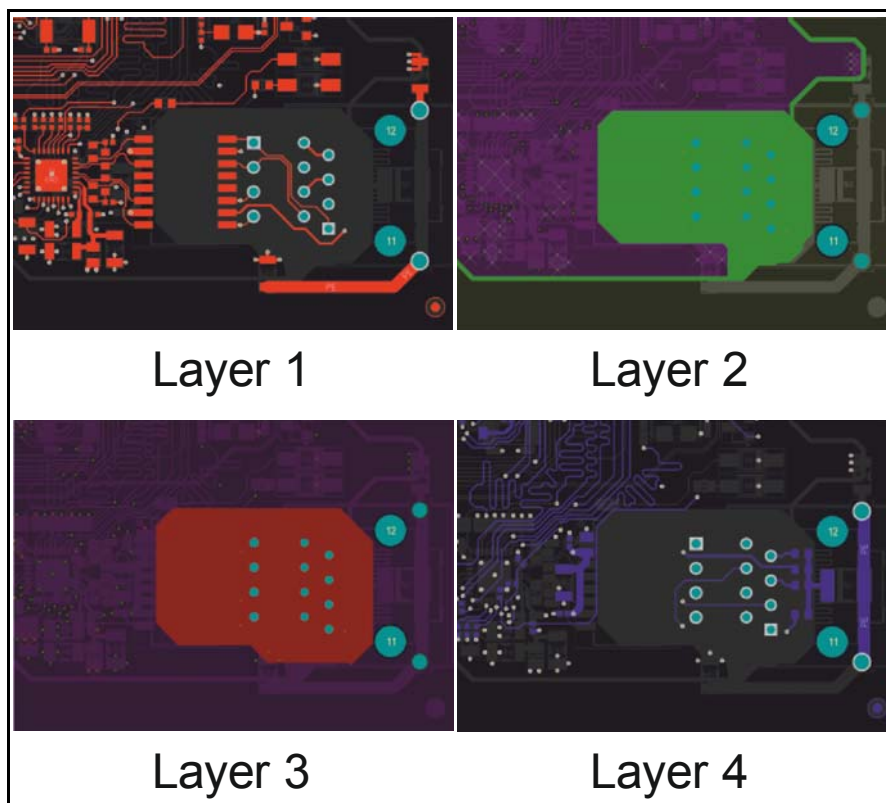

Figure 4: A single layer view of the PCB in Figure 3

So what does all this mean for the PCB layout in particular?

- In order to comply with the standard carefully keep the creepage and clearance distance that is required to comply with IEC60950-1. The creepage distance on PCBs does depend on the selected pollution degree. Usually pollution degree is 2 "which applies where there is only non-conductive pollution that might temporarily become conductive due to occasional condensation". Pollution degree 1 "applies where there is no pollution or only dry, non-conductive pollution". This means hermetically sealing of the PCB or conformal coating (solder resist is not conformal!). Creepage distance depends on the working voltage which is determined as described in IEC60950-1:2005 clause 2.10.2. The creepage usually is no problem in Ethernet networks since its RMS working voltage is in the SELV range. However the clearance and the transformer insulation are - since it depends on the peak working voltage and the maximum peak voltage of the transients. Determining the clearance can be done from Annex G of EN60950. Care must be taken when using an un-earthed d.c. mains supply. If it's in the same building the transient voltage on the **d.c. supply line** is assumed to be 71V peak, if it's within the EUT "it shall be in accordance with 2.6.1 e)" (EN60950-1:2005 annex G.2.2) which means that if circuits – in case of a single failure – rely on a connection to Protective Earth in order to reduce transients must be reliable connected to PE. From the 1500V requirement as explained above (which assumes the Ethernet connection to be a TNV-1 or TNV-3 circuit (see IEC60950-1:2005, clause 2.3 and annex G 3). In accordance to table G.2 in annex G.6 for equipment that is used below 2000m above sea level the minimum clearance (reinforced insulation) is 1.6mm for all pollution degrees. Please read annex G.6 carefully because there are exceptions.
- Isolation of the transformer must also withstand 1500V RMS for a t least 60s. And this is also true on PCBs for the isolation to a GND plane. This is regulated in 2.10.6.4 of IEC60950-1:2005. So the best is to cut out all copper planes below the transformer and the connector.
- Special care must be taken on the dielectric strength of the capacitor from the Bob Smith Termination (we will discuss that later) to chassis which shall be 2KV.

To ease your pain you can use a connector with integrated magnetics and integrated termination. Those are available from a variety of vendors.

2.2.3 Electromagnetic Interference

Compliance with EMI regulations is always an issue with high speed interfaces and neglecting the basics of a high speed PCB design is a guaranty to fail. Before you go to the EMC lab for testing you have to determine if you device is an industrial (Class A) or residential, commercial or light industrial device (Class B). For Class A devices the emission requirement is lower but the immunity requirement is higher and vice

versa for Class B devices. I normally recommend to test the heavier requirement for both, Class A and Class B so that the device meats both criteria.

For radiated and conducted emission it is essential that no common mode signal can run over the Ethernet cable and use it as a resonant antenna (standing wave on the cable). This is directly related to the quality of the magnetics. They should have a common mode choke on the line side and a good common mode balance is also mandatory. The common mode choke cannot be on the PHY side since most PHYs can only sink current and therefore need a center tap to feed the transformer with a positive voltage. Any imbalance here causes common mode current to travel over the cable causing radiation. Also the quality of the cable has an impact. The Bob Smith termination of the cable reduces the common mode radiation. Although not being optimal it is widely used. "Bob Smith described in his patent (U.S. Patent, 5,321,372 issued 6/14/94) a method to reduce the longitudinal or common mode current on multipair conductor systems where the pairs are interrelated in a uniform manner. He alludes to the fact that the pair to pair relationships of a CAT5 cable form transmission lines in themselves [12]. As Jim points out in his Engineer's Notes Bob Smith seemed to calculate an impedance of about 145 ohms which hey says is wrong. As a result terminating the cable with about 52.3 ohms instead of Bob Smith's 75 ohms can improve the return loss significantly.

Since radiation can also be caused by the rest of the circuit and then coupling into the cable in the near field care should also be taken on a correct PCB layout (see Chapter xx about Signal Integrity). Of course radiation is also influenced by the shielding of the cable and the enclosure. Shielding can be considered a elongating the enclosure over the cable. If any modulated current flows over the shield (if one is used) it acts as an antenna itself. This can happen due to potential differences on each end of the cable. Proper low impedance attachment of the shield to earth is important.

2.2.4 10Base-T and 100Base-TX in particular

2.2.4.1   10Base-T

10Base-T is the Ethernet standard for transmission of 10 Mbit over an unshielded twisted pair cable which can have a length of max. 100m. Transmitter and receiver hereby are using different pairs. Only a point-to-point connection is possible (e.g. a maximum of two MAUs can be connected per segment. Due to the CSMA/CD the signal travelling time is limited and therefore the maximum length of a network is limited to 2500m. CSMA/CD means Carrier Sense Multiple Access which means that a station tests if there is no other signal at the link before it starts sending and Collision Detection which means that since CSMA is not enough to prevent a collision the collision is detected and the station then waits a random time before it tries to send again.

It is obvious that in a network that does not connect multiple links by means of a hub a full duplex operation is possible without any collision and therefore the CSMA/CD mechanism is not necessary (see also IEEE 802.3-2008, 1.1).

The electrical specification of the signal is as follows (see 802.3-2008, 14.3):

- The transmitter shall meet all requirements when connected to a load of 100 ohms
- For measurement a model for the twisted pair cable is used as described in Fig. 14-7 of IEEE 802.3-2008
- The peak differential voltage of the transmitter shall be between 2.2V and 2.8V when terminated with 100 ohms
- The transmitter shall provide equalization so that the output waveform falls within the template shown below for all transmitted data sequences (this means the eye diagram). Therefore the twisted pair model is used and the transmitter is connected through a balun. The transmitter is driven by a pseudo random Manchester code sequence with a minimum repetition period of 511 bits
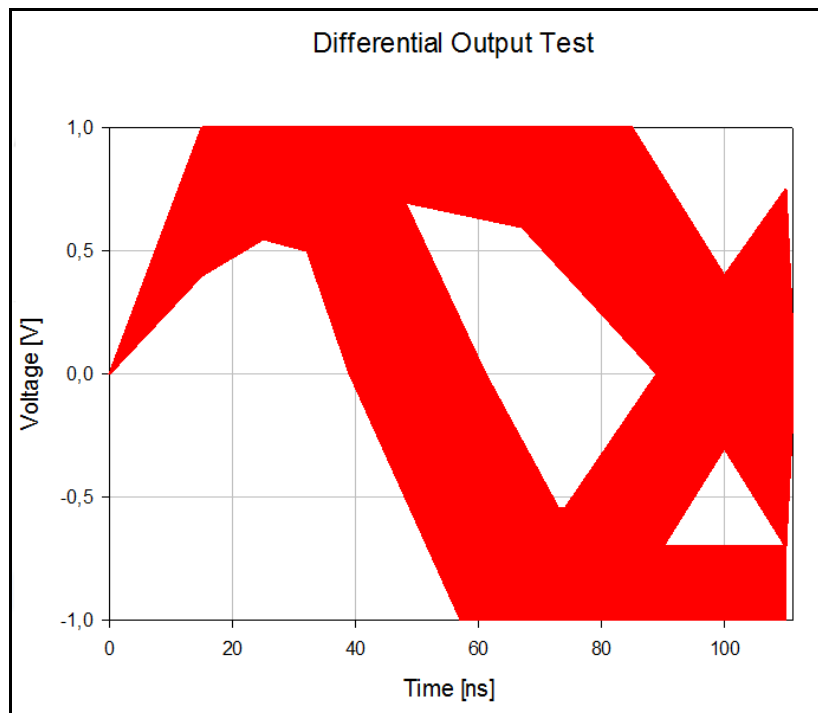
Figure 5: Mask for differential output test for a 10Base-T signal

- When no data is sent the MAU sends and idle signal (see waveform below) followed by an repeated 16ms +/-8ms period of silence and a link test pulse
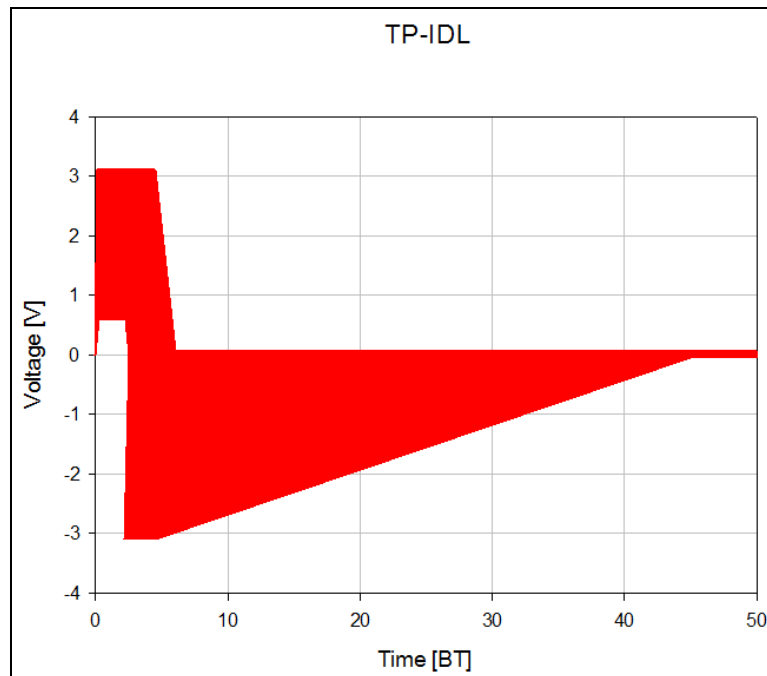

Figure 6: Idle Pulse Mask for a 10Base-T signal

- Before the link is established the MAU only sends link test pulses (see waveform below). The receiving MAU monitors the receive line either for idle and link test pulses or incoming data. If none is received for a time between 50ms and 150ms the MAU enter the Link Test Fail state which is left when a number of link test pulses (between 2 and 10) are received.
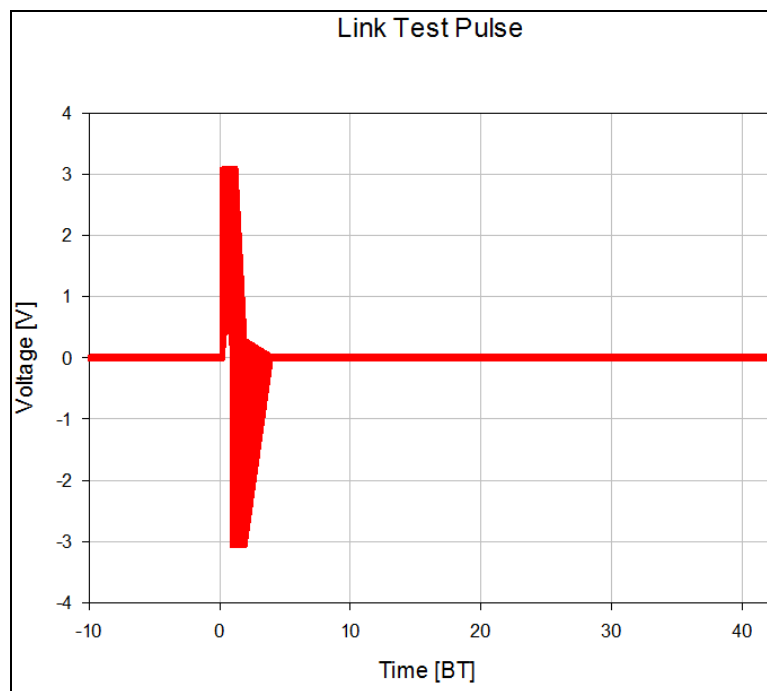
Figure 7: Link Test Pulse Mask

- It is strongly recommended that Autonegotiation is used to determine either half or full duplex mode and the bit rate (10Base-T or 100Base-T).

Since the receiver needs to synchronize to the clock of the transmitter and there is no separated clock line the clock needs to be recovered by means of a PLL from the data. To accomplish that a special coding is used to guarantee either synchronizing of the receiver PLL and keep it locked while a packet is received:

The MAU uses Manchester Coding to send the data. This means that the signal will change its state in the middle of a data bit. A falling edge defines a logical 1 and a rising edge define a logical 0 (the originally defined Manchester Code does it vise versa). Using Manchester coding also provides us with a DC bias free line signal. The disadvantage of the Manchester Coding is that the bandwidth is doubled.

For synchronization an Ethernet packet (Ethernet frame) as defined on the Logical Link Layer (Layer2, the MAC layer) starts with a 7 byte preamble of hex AA followed by a start of frame delimiter (one byte, hex AB). Then the rest of the frame follows.

2.2.4.2   100Base-TX

100Base-T or Fast Ethernet comes with a family of 100Mb/s physical layers which either uses an electrical or optical interface allowing only two participants per segment. We only discuss the 100Base-TX interface (electrical, dual twisted pair). The physical layer relates to ANSI INCITS 263-1995 (S2010) standard for Fiber Distributed Data Interface (FDDI) and Token Ring Twisted Pair Physical Layer Medium Dependent (TP-PMD). The coding of 100Base-TX is completely different from the cod-

ing used for 10Base-T: The MDI uses MLT3 coding on the line which means that a1 is encoded as a change of level and a 0 is encoded as no change. MLT3 uses three levels of logic (ternary signal), named (+,0,-). Since in a sequence of logic 1's the level changes are in the fixed order (0, +, 0, -) the bandwidth of the signal is only ¼ of the NRZ input before encoding. The Problem is that for a sequence of 0's there is no level change and therefore a clock recovery is not possible. To overcome this the original input on a byte level is separated in two 4bit nibbles and each nibble passes a 4B5B-Encoder which ensures that there is no sequence of five 1's or five 0's. In addition now also special signal (called k-characters) are available which can be used for synchronization and signaling. The 4V5B-Coding increases the NRZ-Bitrate of 100Mb/s to 124Mb/s. Therefore the maximum bandwidth is 125MHz x ¼ = 31.25MHz.
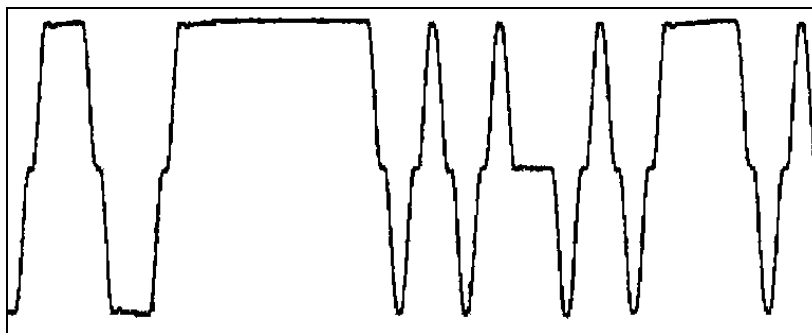

Figure 8: Typical MLT-3 Signal

According to ANSI INCITS 263-1995 there are requirements regarding that signal which can be summarized as follows:

Characteristics	Minimum	Maximum	Units
Differential Signal, UTP, zero-peak	950	1050	mVpk
Differential Signal, STP, zero-peak	1165	1285	mVpk
Signal Amplitude Symmetry (pos./neg.)	98	102	%
Rise and Fall Time	3.0	5.0	ns
Rise and Fall Time Symmetry	0	0.5	ns
Duty Cycle Distortion, peak-to-peak	0	0.5	ns
Transmit Jitter (HLS)	0	1.4	ns
Overshoot	0	5	%

Table 2: Twisted Pair Output Interface characteristics

The requirement for the waveform overshoot also requires that "any overshoot or undershoot transient shall have decayed to within 1% of the steady state voltage within 8ns following the beginning of the differential signal transition".
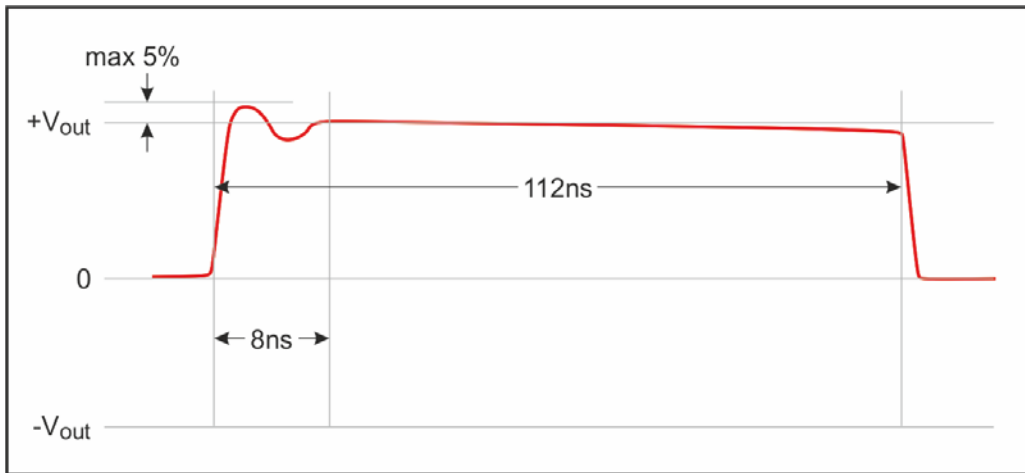
Figure 9: Active Output Interface Overshoot

Also the signal droop is limited. Since Baseline Wander Tracking of the receiver depends on the droop the worst case droop is limited. The droop is directly related to the transformers open circuit inductance (OCL). ANSI INCITS 263-1995 therefor requires a minimum worst case OCL of 350µH with any DC bias current between 0mA and +8mA.

Table 2 does not show the Return Loss requirement. The Interface shall meet the Return Loss requirements below for any specified line impedance:

- Greater than 16dB from 2MHz to 30MHz
- Greater than $(16 - 20 \log (f / 30\text{MHz}))$dB from 30MHz to 60MHz
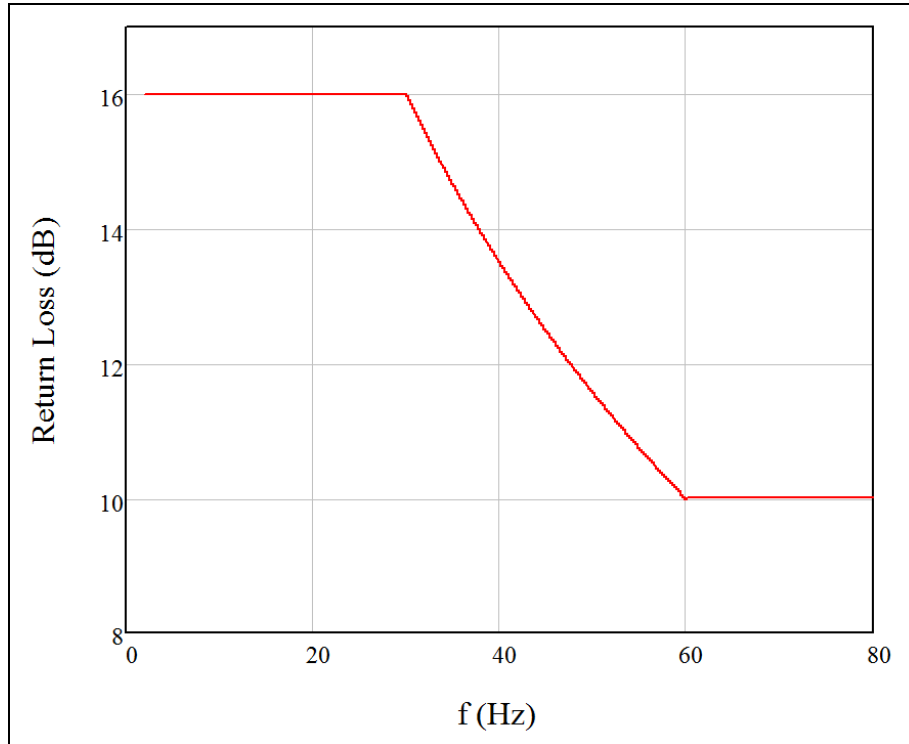- Greater than 10dB from 60MHz to 80MHz

Figure 10: Return Loss of Active Output Signal

The Rise/Fall times are defined as the time from 10% of the signal amplitude to 90% of the signal amplitude.
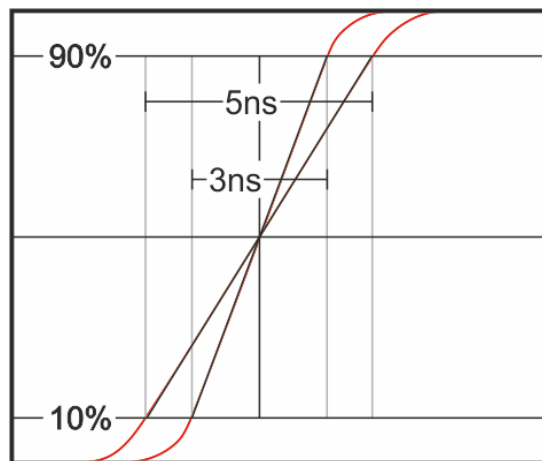

Figure 11: Minimum and maximum rise time

The maximum duty cycle distortion is defined as the maximum deviation from a time difference of 16ns between the 50% amplitude values of the signal when fitted to a 16ns time grid.

Figure 12: Duty Cycle Distortion

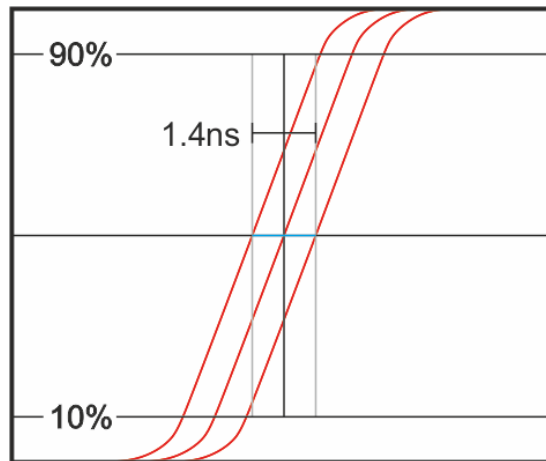The maximum jitter requirement means peak to peak jitter (6σ).

Figure 13: Maximum Peak-toPeak Jitter

Summarizing all requirements, a simple eye pattern mask test can be defined. Though it is not mandatory it easily lets you qualify a 100Base-TX signal. A lot of common oscilloscopes nowadays are capable of performing the tests as described above using a differential active probe and a special software.
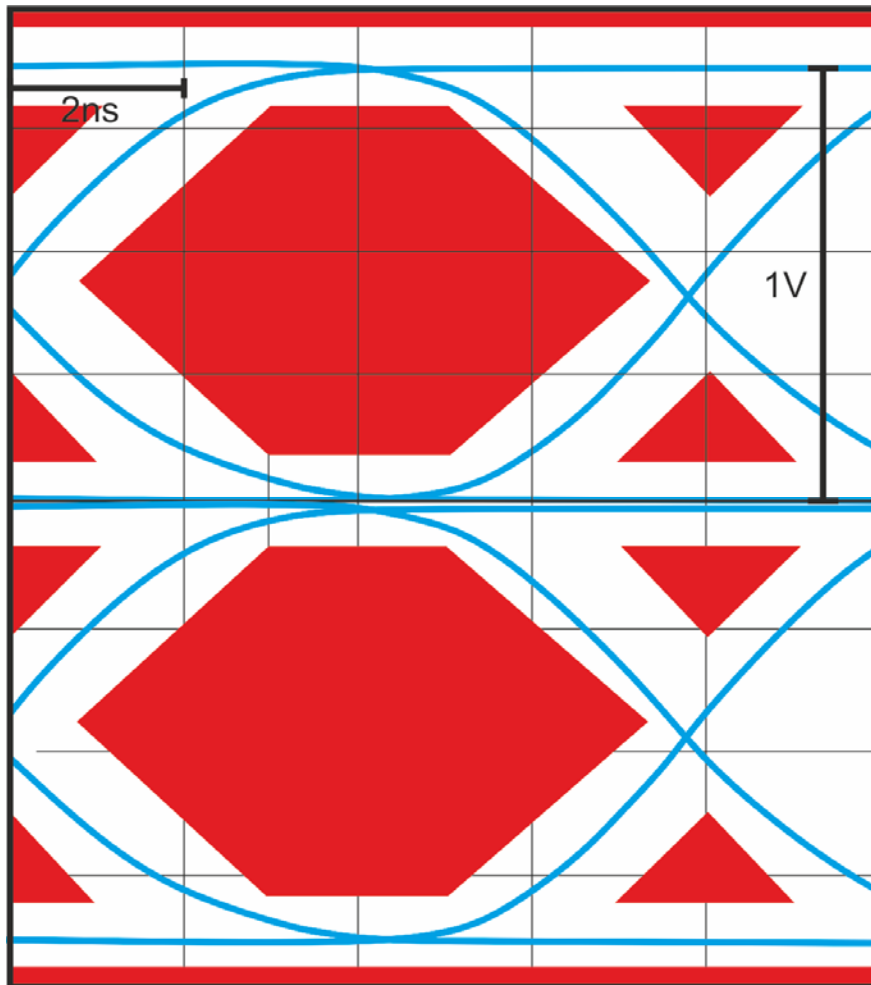
Figure 14: Mask definition for Eye Pattern Test (see Annex J of ANSI INCITS 263-1995

Since it should be possible to connect a legacy 10Base-T device to 100Base-TX segments it is strongly recommended that the PHY is capable of recognizing whether a 10Base-T or 100Base-TX device is connected to it and switch to the correct physical layer. This mechanism is called autonegotiation. In 100Base-TX segments the normal link pulse (NLP) is replaced by a fast link pulse (FLP). It is also transmitted every 16ms (+/-8ms) as the 10Base-T NLP. The 10Base-T PHY recognizes a NLP when receiving an FLP and therefore they assume a link but they are not capable of recognizing the information coded in the FLP. Each FLP has a duration of 100ns (as well as the NLP pulse) but the single NLP pulse is replaced by a burst of a maximum of 97 evenly spaced 100ns pulses. The pulse to pulse time is typ. 62.5µs. The odd pulses are the clock pulses and the even pulses are the data pulses. Omitting a data pulse means a logical 0 while a logical one means that the data pulse is present. For a detailed description see IEEE 803.3-2008, clause 28.

2.3 The Media Independent Interface

2.3.1 The normal MII interface

Having discussed the media dependent interfaces physics we now have a closer look at the media independent interface which connects the PHY to the MAC. The relationship to the OSI reference model is shown in IEEE 803.3-2008, clause 22.1.
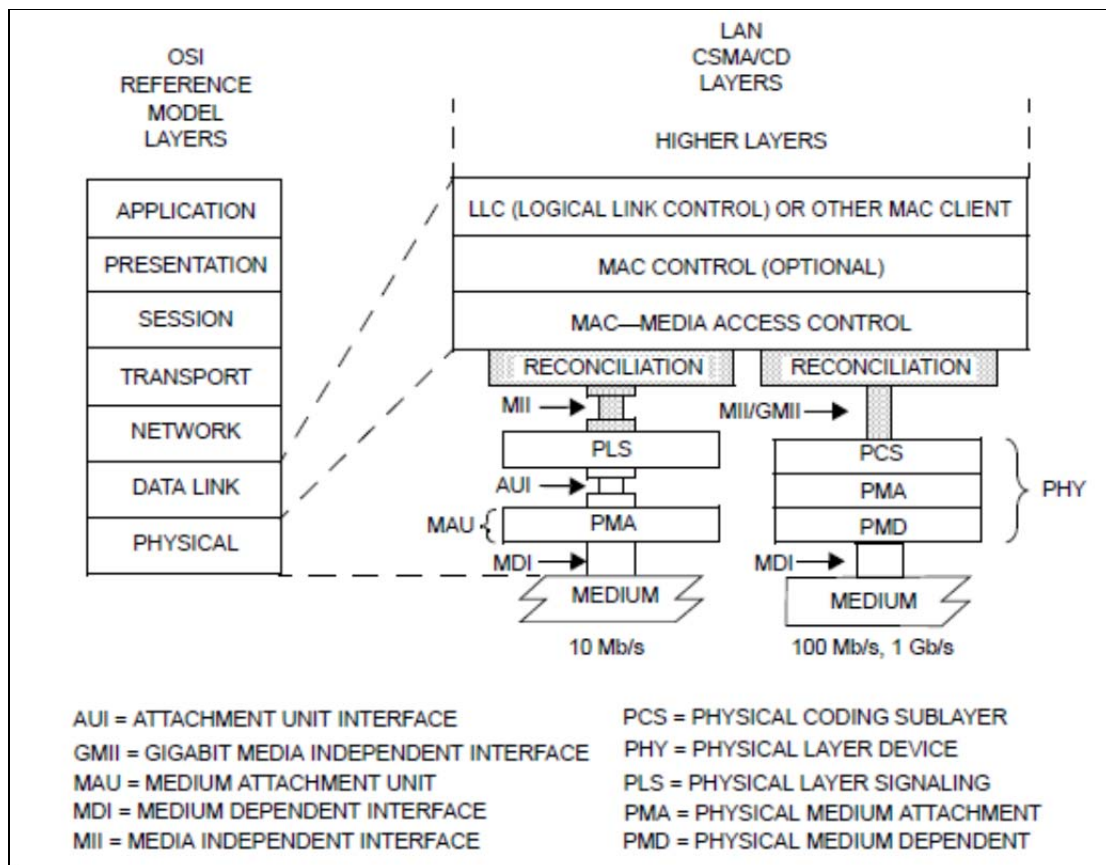

Figure 15: MII relationship to the ISO/IEC Open System Interconnection (OSI) reference model and the IEEE 802.3 CSMA/CD LAN model (from IEEE 803.3-2008)

The Reconciliation Sublayer is the logical part of the interface between the MAC and the PLS and the MII is the physical part. Although the MII interface is capable of driving a shielded cable it normally resides directly on the PCB.

The signals use TTL signal levels and therefore are interoperable with 3.3V and 5V logic (please verify if a 3.3V device does really tolerate 5V inputs. As an example the DAVICOM DM9161C does).

The MII interface is a synchronous interface with a clock frequency of nominally 25MHz. The interface uses 4 data lines to transmit and receive data. The PHY sources the clock for the transmit and receive part of the interface.

The following figure gives an overview of the signals of the MII interface and the mapping between MII signals and PLS service primitives.
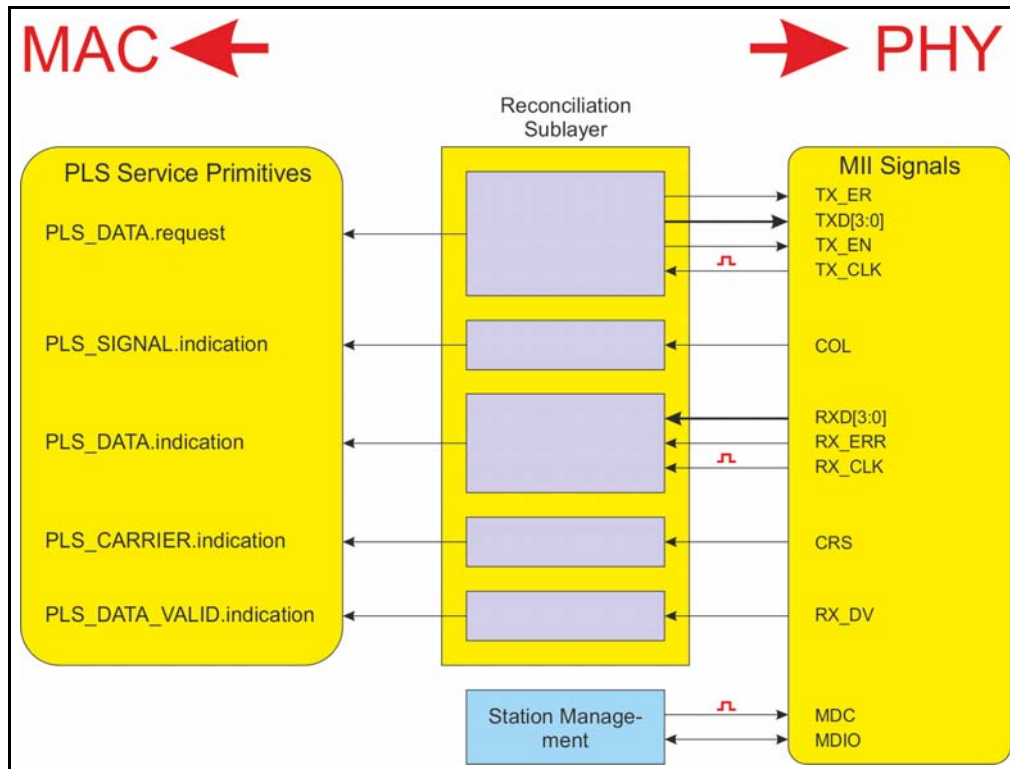
Figure 16: Reconciliation Sublayer (RS) inputs and outputs and STA connection to MII (from IEEE 803.3-2008)

In order to implement the interface on a PCB or using a shielded cable it is crucial to meet all electrical requirements of the interface and have a look at the signal integrity. We will not discuss connecting multiple PHYs to a MAC although this is possible but only a point-to-point connection since in most applications only one PHY is attached.

Since the MII interface uses TTL thresholds the following applies:

Signal	Minimum	Maximum
Output logic high level (V_{OH}), I_{OH} = -4mA	2.4V	V_{cc}
Output logic low level (V_{OL})), I_{OL} = 4mA	0V	0.4V
Input logic high level (V_{IH})	2V	V_{cc}
Input logic low level (V_{IL})	0V	0.8V
Input high current I_{IH} (V_I = 5.25V) (all except COL, MDC, MDIO)	-	200µA
Input high current I_{IH} (V_I = 5.25V) (COL, MDC, MDIO at input of PHY)	-	20µA
Input high current I_{IH} (V_I = 5.25V) (MDIO at input of STA)	-	3000µA
Input low current I_{IL} (V_I = 0V) (all except COL, MDC, MDIO)	-20µA	-
Input low current I_{IL} (V_I = 0V) (COL at input of RC sublayer)	-200µA	-
Input low current I_{IL} (V_I = 0V) (MDC at input of PHY)	-20µA	-

|		
Input low current I_{IL} (V_I = 0V) (MDIO at input of STA)	-180µA	-
Input low current I_{IL} (V_I = 0V) (MDIO at input of PHY)	-3800µA	-
Input quiescent current I_{IQ} (V_I = 2.4V) (MDIO at input of STA)	-	1450µA
Input quiescent current I_{IQ} (V_I = 2.4V) (MDIO at input of PHY)	-1450µA	-

Table 3: DC characteristics of MII signals

The input capacitance for all signals other than MDIO shall not exceed 8pF. For the MDIO signal the input capacitance shall not exceed 10pF.

If using a twisted pair cable for connection the single ended impedance shall be 68Ω +/-10% (using one conductor of the pair as the return conductor). The propagation delay of the cable shall not exceed 2.5ns.

However if you design the interface on a PCB will more have to deal with transmission lines with an impedance between 50Ω and 60Ω.

At least for the clock signals it is mandatory to avoid double triggering due to over/undershoot or superposition of the reflected wave. Although there is no hint for the needs of an external series resistor in DAVICOMs application circuits (IEE 802-3-2008 requests this if necessary) I recommend placing a series resistor for the clock lines to adapt the driver's output impedance to the impedance of the transmission line and determine the series resistor value by measurement (22Ω is a good starting value for a 3.3V device; check also Annex 22B.1 of IEEE802-3-2008). If the resistor is not needed then populate 0 Ω.
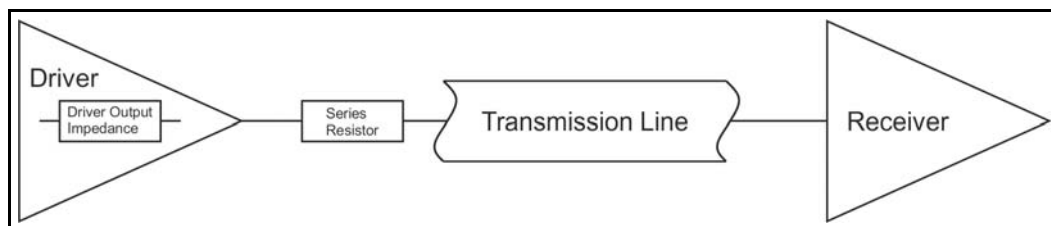
Figure 17: Typical PCB connection between driver and receiver.

If insufficient series termination is used the reflected wave can cause double triggering if it passes through switching threshold of the receiver. IEEE802.3-2008 (Clause 22.4.3.2) states: "The initial incident potential change arriving at the receiving end of a point-to-point MII signal path plus its reflection from the receiving end of the path must switch the receiver input potential monotonically from a valid high (one) level to Vil ≤ Vil(max) – 200 mV, or from a valid low (zero) level to Vih ≥ Vih(min) + 200 mV. Subsequent incident potential changes arriving at the receiving end of a point-to-point MII signal path plus their reflections from the receiving end of the path must not cause the receiver input potential to reenter the range Vil(max) – 200 mV < Vi <

Vih(min) + 200 mV except when switching from one valid logic level to the other. Such subsequent incident potential changes result from a mismatch between the characteristic impedance of the signal path and the driver output impedance."

This means that

1. The Receiver switches on the superposition of the incident wave and the reflected wave. Since the receiver has a high input impedance the reflection coefficient is 1. The strip line and the driver output resistance form a voltage divider and the incident wave has a potential of $V_{out}/2$. The reflected wave also has a potential of $V_{out}/2$ due to the reflection coefficient and superposition of both waves sum up to a potential of V_{out}.
2. Subsequent potential changes and reflections shall not enter the forbidden range of V_{IL}-200mV to V_{IH}+200mV.
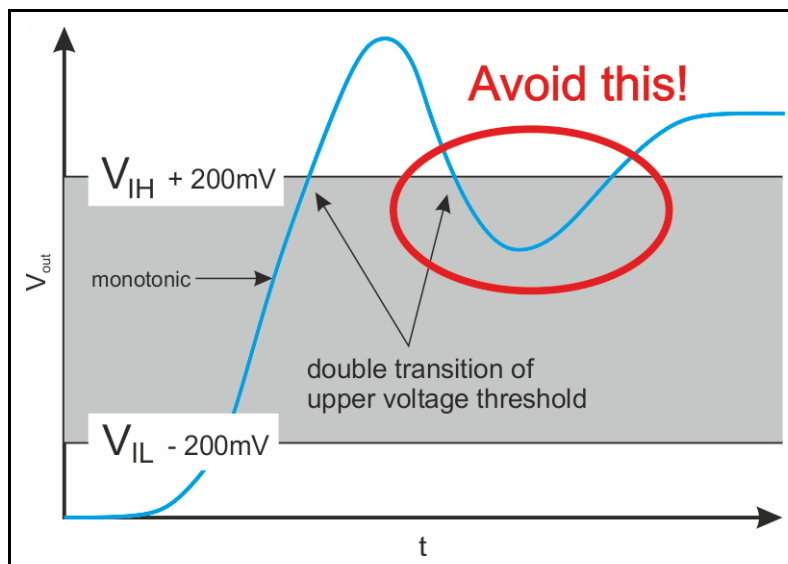

Figure 18: Double switching caused by superposition of the reflected wave

Now let's have a closer look at the signals of the MII interface:

Signal	Function
TX-CLK	The continuous transmit clock is the timing reference for RX-DV, RXD[3.:0] and RX-ER. It is sourced by the PHY and has a nominal frequency of 25MHz (at 100Mbit/s) and 2.5MHz (at 10Mbit/s) (25% of the nominal transmission rate). The duty cycle is between 35% and 65% and the frequency deviation shall be no more than ±100ppm
RX-CLK	The continuous transmit clock is the timing reference for TX-EN, TXD[3.:0] and TX-ER. It is sourced by the PHY and has a nominal frequency of 25MHz (at 100Mbit/s) and 2.5MHz (at 10Mbit/s) (25% of the nominal transmission rate of 100Mbit/s). The duty cycle is between 35% and 65%. A guaranteed phase relationship between TX-CLK and RX-CLK is not required.

TX-EN	Indicates that the RC sublayer is presenting valid nibbles (on TXD[3:0]). It is asserted synchronously with the first nibble of the preamble and remains asserted until all nibbles have been sent. Deassertion takes place prior to the first TX-CLK following the last nibble. TX-EN is an input of the PHY
TXD[3:0]	These signal lines present the data nibbles on the MII interface. They are an output of the PHY and transition synchronously with respect to TX-CLK. TXD[3:0] are only valid when TX-EN is asserted. TXD[0] is the least significant bit of the data nibble. TXD[3:0] are inputs of the PHY.
TX-ER	TX-ER signals a transmit coding error and is an input of the PHY. It transitions synchronously with respect to TX-CLK. While TX-ERR and TX-EN is asserted the MAC transmits one or more symbols that are not part of the valid data. In 10Mbit/s mode the signal is ignored
RX-DV	RX-DV is an output of the PHY. It indicates that valid data is presented on RXD[3:0].
RX-ERR	RX-ERR is an output of the PHY and signals a coding error to the RC layer (or any error that the PHY can detect). RX-ERR is only valid while RX-DV is asserted.
CRS	CRS is the carrier sense signal and is an output of the PHY. It is asserted when either the transmit or receive medium is nonidle. It is deasserted when both the transmit and receive media are idle. CRS also remains asserted throughout the duration of a collision condition. CRS is not required to be synchronous to TX-CLK or RX-CLK.
COL	COL is an output of the PHY and signals a collision on the medium. It remains asserted while the collision persists. COL is not required to be synchronous to TX-CLK or RX-CLK.
MDC	MDC is sourced by the station management entity of the MAC and is an input of the PHY. It is the timing reference for the transfer of information on the MDIO signal. MDC is aperiodic and has no maximum high or low times. The minimum high and low times for the MDC signal are 160ns each and the minimum period is 400ns. DM9161C for instance allows a period of 80ns here.
MDIO	MDIO is a bidirectional signal that is used to transfer control information and status between PHY and STA. It is driven and samples synchronously with respect to MDC

Table 4: Signals of the MII interface

Since we will concentrate on the physics of the interface we will not describe the protocol used on the MII interface here. Please refer to IEEE802.3-2008 clause 22.2.3 and 22.2.4.

Let's have a look at the timing of the signals: All synchronous signals of the MII interface are related to a clock edge. Output signals have a clock-to-output delay from the clock edge they refer to until they are valid (t_{CO}). All input signals need a minimum

setup time from the time they are valid until the clock edge they reference to (t_{SETUP}) and a minimum hold time they must be valid after the clock edge (t_{HOLD}).
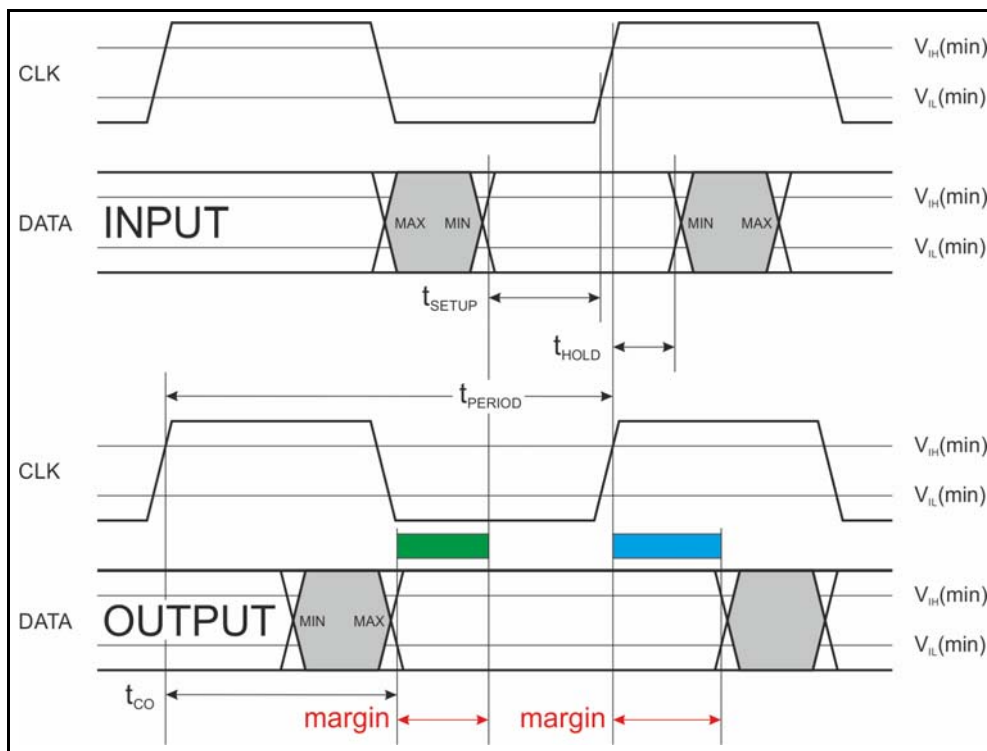

Figure 19: Timing of synchronous signals

Signal	Clock To Output	Setup Time	Hold Time	Clock Edge
TXD[3:0]	Min 0ns Max 25ns			TX-CLK rising
TX-EN	Min 0ns Max 25ns			TX-CLK rising
TX-ER	Min 0ns Max 25ns			TX-CLK rising
RXD[3:0]		Min 10ns	Min 10ns	RX-CLK rising
RX-DV		Min 10ns	Min 10ns	RX-CLK rising
RX-ER		Min 10ns	Min 10ns	RX-CLK rising
MDIO	Min 0ns Max 300ns	Min 10ns	Min 10ns	MDC rising

Table 5: Signal timing as specified in clause 22.3 of IEEE 802.3-2008

Since IEEE 802.3-2008 only specifies one side of the interface (e.g. for signals related to TX-CLK only the t_{CO} of the transmitter is defined and the t_{SETUP} and t_{HOLD} of the receiver is not you should check the timings of the PHY and the MAC from their datasheets carefully. In the following we will do that for one of Freescale's Kinetis processors and Davicom's DM9161C PHY.
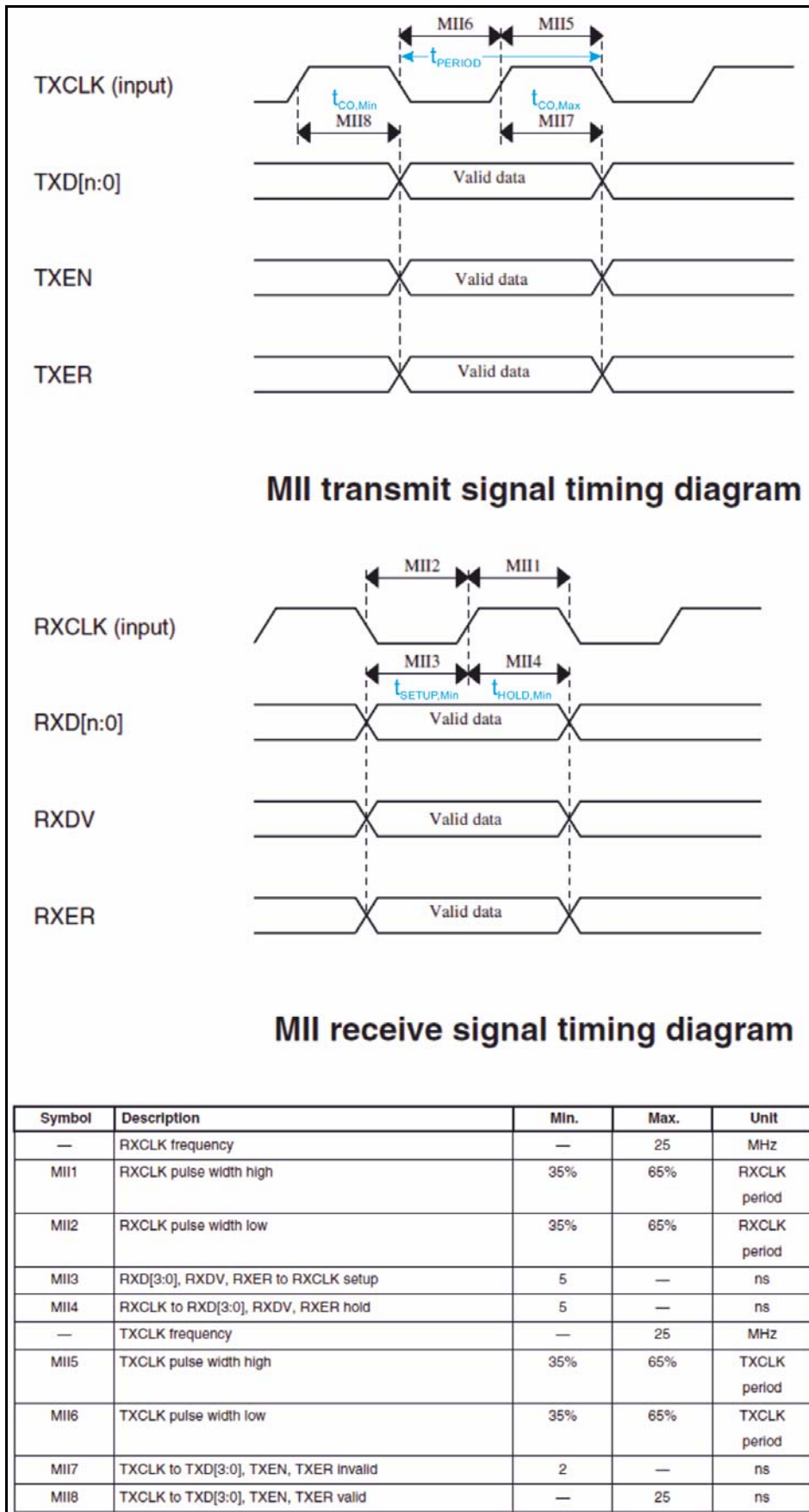
MII transmit signal timing diagram

MII receive signal timing diagram

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

Figure 20: MII switching characteristics of Freescale's MK60DN512ZVLQ10

The MII timing specification of the processor must be compared to the timing specification of the PHY.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tTXc	TXCLK Cycle Time	39.9988	40	40.0012	ns	30ppm
tTXh, tTXl	TXCLK High/Low Time	16	20	24	ns	
tTXs	TXD [0:3], TXEN, TXER Setup To TXCLK High	12	-	-	ns	
tTXh	TXD [0:3], TXEN, TXER Hold From TXCLK High	0	-	-	ns	
tTXOD	TXCLK to Output Delay			25	ns	
t1	TXEN Sampled To CRS Asserted	-	4	-	BT	
t2	TXEN Sampled To CRS De-asserted	-	4	-	BT	
tTXpd	TXEN Sampled To TX+/- Out (Tx Latency)	-	8	-	BT	
tTXr/f	100TX Driver Rise/Fall Time	3	4	5	ns	90% To 10%, Into 100ohm Differential

Note 1. Typical values are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
tRXc	RXCLK Cycle Time	39.9988	40	40.0012		30ppm
tRXh, tRXl	RXCLK High/Low Time	16	20	24		
tRXs	RXD [0:3], RXDV, RXER Setup To RXCLK High	10	-	-	ns	
tRXh	RXD [0:3], RXDV, RXER Hold From RXCLK High	10	-	-	ns	
tRXpd	RX+/- In To RXD [0:3] Out (Rx Latency)	-	15	-	BT	
t1	CRS Asserted To RXD [0:3], RXDV, RXER	-	4	-	BT	
t2	CRS De-asserted To RXD [0:3], RXDV, RXER	-	0	-	BT	
t3	RX+/- In To CRS Asserted	10	-	14	BT	
t4	RX+/- Quiet To CRS De-asserted	14	-	18	BT	
t5	RX+/- In To COL De-Asserted	14	-	18	BT	

1. Typical values are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Figure 21: MII-Timing of DM9161C

Please notify that for the RX-Timing of the PHY a setup and hold time is specified. Since RXD[3:0] for instance, is an output of the PHY the clock-to-output time is required and this is derived from those timings (see Figure 21).

2.3.2 The RMII interface

The RMII interface has been established by the RMII consortium. The actual release of the specification is from 1997 and can be downloaded from National Semiconductor's website (http://www.national.com/assets/en/other/rmii_1_2.pdf). The interface reduces the number of data lines and control lines but doubles the clock frequency.

Most of the tables and figures in the following paragraphs are taken from the RMII specification without explicit notification.
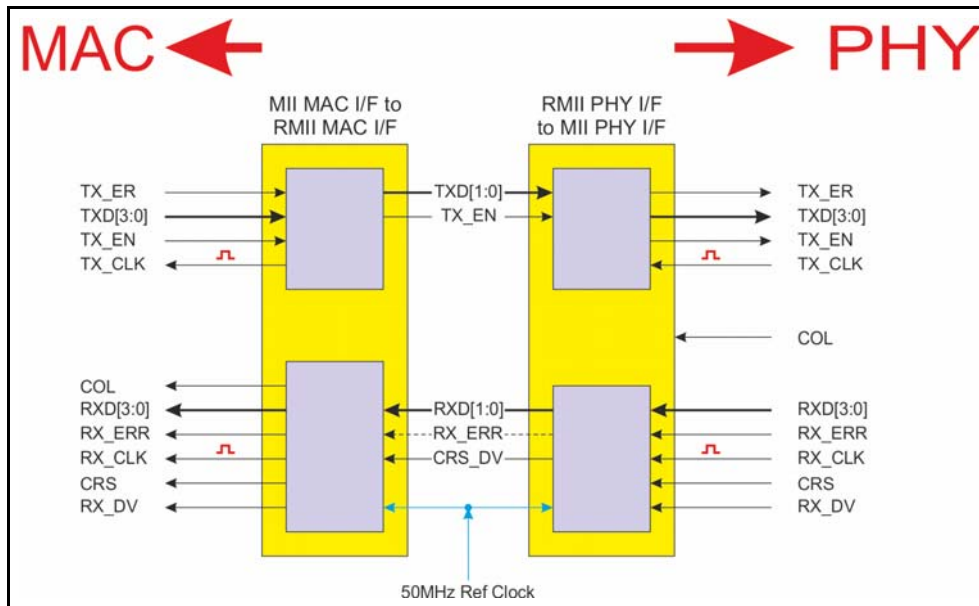
Figure 22: Signal Reconciliation Map of the RMII interface

The RMII signal definition is as follows:

Signal Name	Direction (with respect to the PHY)	Direction (with respect to the MAC)	Use
REF_CLK	Input	Input or Output	Synchronous clock reference for receive, transmit and control interface
CRS_DV	Output	Input	Carrier Sense / Receive Data Valid
RXD[1:0]	Output	Input	Receive Data
TX_EN		Output	Transmit Enable
TXD[1:0]		Output	Transmit Data
RX_ER	Output	Input (not required)	Receive Error

Table 6: RMII Specification Signals

The reference clock is a continuous clock that is either sourced by the MAC or an external source (clock distribution device). The reference clock shall be 50MHz ±50ppm with a duty cycle between 35% and 65%. The PHY shall use the reference clock as the network clock.

CRS_DV shall only be asserted by the PHY when the medium is nonidle. It is asserted asynchronously on detection of carrier. Loss of carrier shall result in a deassertion of CRS_DV synchronous to the reference clock. RXD[1:0] is valid only when CRD_DV is asserted.

RXD[1:0] and TXD[1:0] transition synchronously to the reference clock. They carry the di-bits of a package received by the PHY resp. a package that should be sent by the PHY.

TX_EN is asserted synchronously with the first nibble of the preamble and remains asserted until all data of the packet is sent. It is negated prior to the first REF_CLK rising edge that follows the final di-bit of a frame. It indicates that the transmit data is valid.

Please notice that the RMII interface – other than the MII interface – uses a single clock for receive and transmit path which can either be source by the MAC or an external clock distribution.

TTL signal levels are used. All inputs shall be able to tolerate input potentials up to 5.5V. All connections are intended to be point-to-point connections on a PCB. If the connections are short paths, transmission line reflections can be ignored. Characteristic impedance or a connector is outside the scope of the RMII specification. I recommend to use impedance controlled transmission lines anyway and to take special care of the clock signal (proper serial termination, we'll discuss this later).

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	$V_I = 5.5V$			200	µA
	I_{IH}	$V_I = 3.6V$			200	µA
Input Low Current	I_{IL}	$V_I = 0.0V$	-20			µA

Table 7: RMII interface DC characteristics

The AC parameters are specified in the following table.

Parameter	Symbol	Min	Typ	Max	Units
REF_CLK Frequency			50		MHz
REF_CLK Duty Cycle		35		65	%
Data Setup Time to rising edge of REF_CLK for TYD[1:0], TX_EN, RXD[1:0], CRS_DV, RX_ER	T_{SU}	4			ns
Data Hold Time from rising edge of REF_CLK for TYD[1:0], TX_EN, RXD[1:0], CRS_DV, RX_ER	T_{HOLD}	2			ns

Table 8: RMII interface AC characteristic

All output drivers shall be capable to drive into a minimum of 25pF while meeting all requirements. This allows about 12 inches of PCB trace. The timing measurement shall be referenced to the point where the reference clock crosses a reference level of 1.4V to the valid input or output at either V_{IL} or V_{IH} level. The rise and fall times shall be measured between V_{IL} and V_{IH} and shall be between 1ns and 5ns.
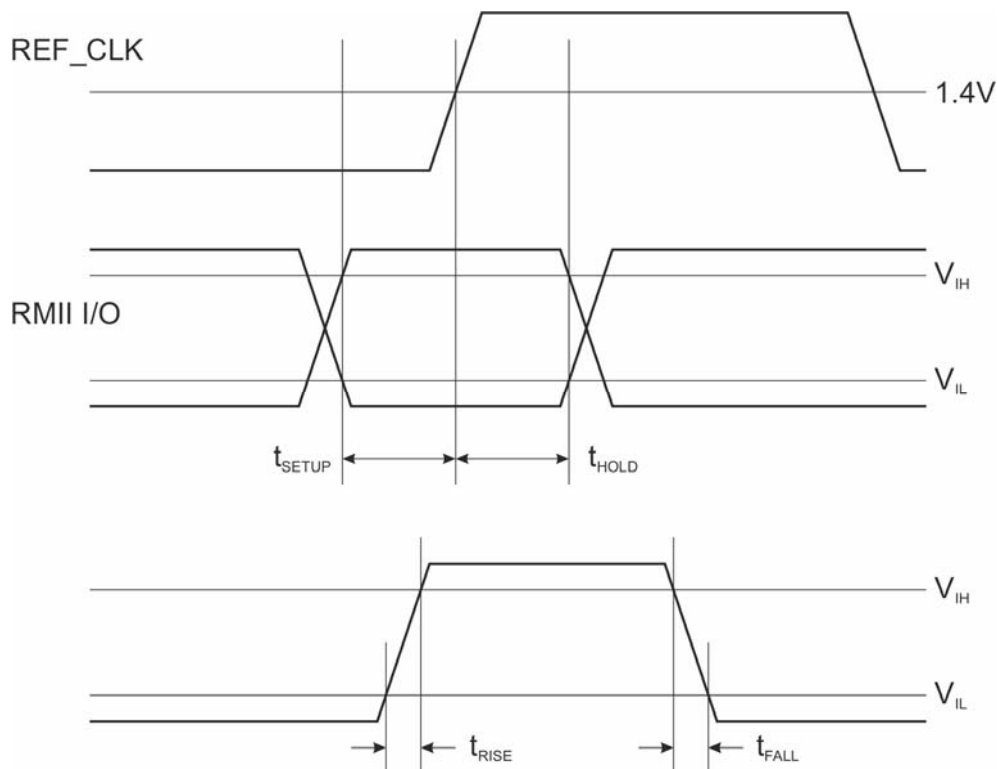
Figure 23: Switching waveforms of MII interface for AC Measurement

3 Technical aspects of implementation

3.1 Signal Integrity

Implementing an Ethernet interface also means taking special care of signal integrity which means that for proper functionality and PCB design a knowledge about behavior of high speed signals is indispensable. Although the clock frequency of the signal may be quite low, the fast rise and fall times of those signals implies harmonics up into the GHz range. These harmonics can also cause radiation if they find an antenna. On a PCB, magnetic loop antennas can also occur if for instance you do not have a contiguous ground plane. For harmonics with a frequency of 1GHz the wavelength on FR4 is about 15cm and a $\lambda/4$ antenna would have a length of about 3.7cm which is in the range of a trace length on the PCB. Poor impedance matching can cause reflections which superimpose the signal and can cause false or double switching, especially of clock lines. An impedance controlled design with a contiguous ground plane therefore is highly recommended.
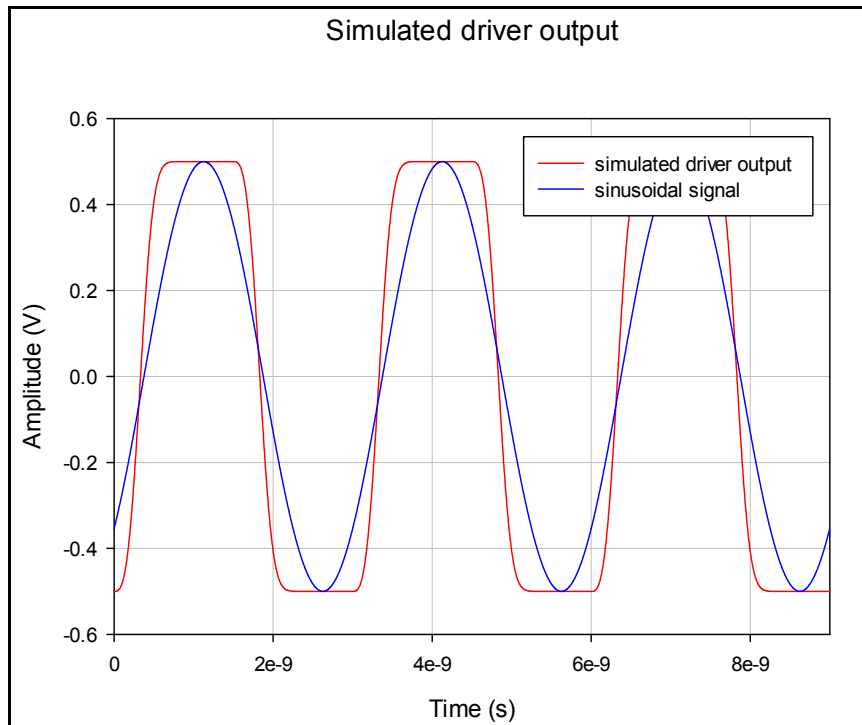
Figure 24: Simulation of a typical driver output and fitted sinusoidal signal
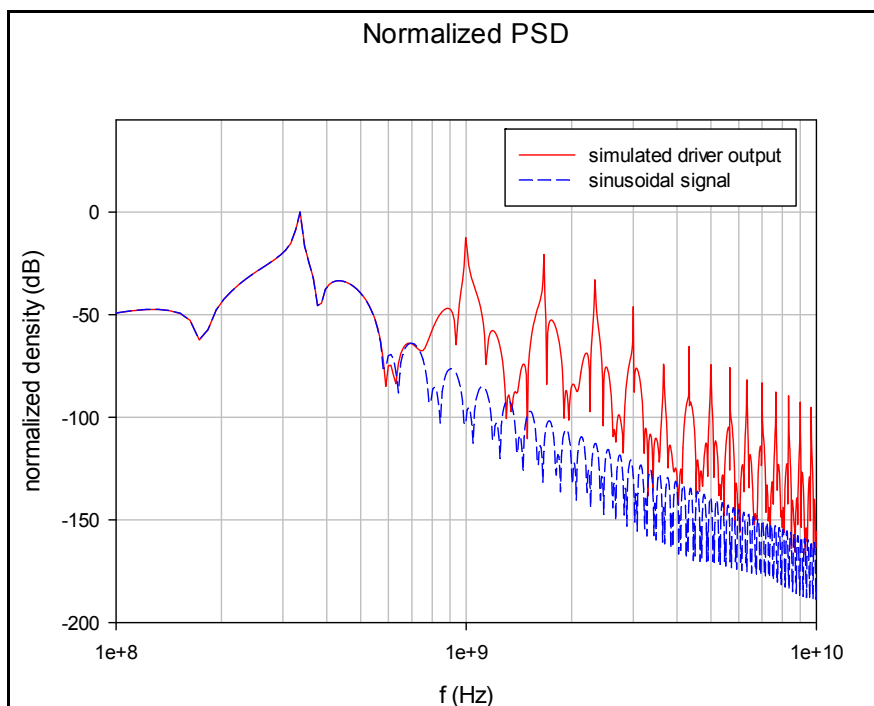
Figure 25: PSD of simulated driver output and sinusoidal signal

As you can clearly see from Figure 25 the more rectangular simulated driver output
has harmonics up to 3GHz (-50dB) compared to the sine signal (Blackman-Harris
Window used before FFT calculation). Those harmonics contribute to the EMI behavior of the device.

3.1.1 Introduction to Transmission Lines

A transmission line is a special structure on a PCB (or a special cable) that is used for point-to-point wiring for high frequency circuits since they have less distortion, less radiation and less crosstalk than an ordinary PCB trace or wire. The transmission line guides a TEM wave from one point to another. As a rule of thumb a PCB trace (or cable) should be treated as transmission line if the wavelength of the conducted ac signal is higher than 10 times the length of the connection. A transmission line can be modeled as a two-port network or quadrupole. An incident wave is transported through the quadrupole while a part of the wave is reflected. This is true for both directions. The amount of conducted and reflected power can be described by means of the Scattering Parameters (S-Parameters).
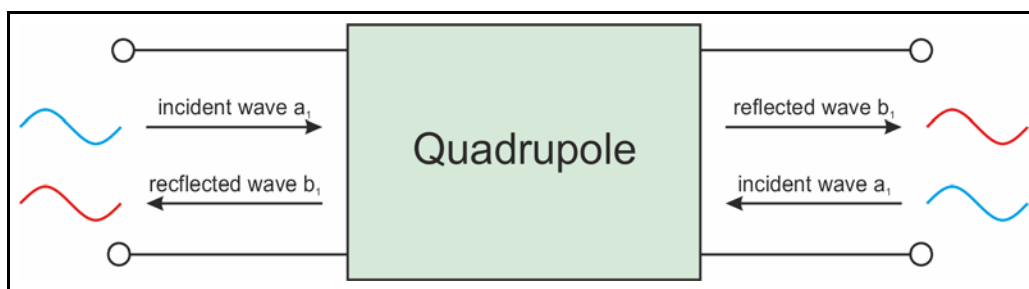
Figure 26: Quadrupole with incident an reflected waves at it's ports

The scattering parameters and the input and output in terms of square root of power form the following matrix equation:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_1 \end{bmatrix} \qquad (3.1\text{-}1)$$

Expanding the matrix yields:

$$b_1 = S_{11}a_1 + S_{12}a_2 \qquad (3.1\text{-}2)$$
$$b_2 = S_{21}a_1 + S_{22}a_2 \qquad (3.1\text{-}3)$$

S_{11} and S_{22} count for the reflection while S_{12} and S_{21} count for the transmission.

- S_{11} is the input port voltage reflection coefficient
- S_{22} is the output port voltage reflection coefficient
- S_{21} is the forward voltage gain
- S_{12} is the reverse voltage gain

The voltage relation results from the convention to write the input and output as square root of the power (see above).

Reflection is caused by impedance mismatch at the input or output of the quadrupole since the transmission line has a characteristic impedance Z_0 where Z_0 is (from Wikipedia: Wave impedance: http://en.wikipedia.org/wiki/Wave_impedance)

$$Z_0 = \frac{E_0^-(x)}{H_0^-(x)}$$

(3.1-4)

which describes Z_0 as quotient of the electric and the magnetic field (in phasor representation). Taking the propagation medium into account this yields

$$Z_0 = \sqrt{\frac{j\omega\mu}{\sigma + j\omega\varepsilon}}$$

(3.1-5)

If the medium is a dielectric (the conductivity is 0) this can be simplified to

$$Z_0 = \sqrt{\frac{\mu}{\varepsilon}}$$

(3.1-6)

The characteristic impedance of free space calculates to

$$Z_0 = \sqrt{\frac{\mu_0}{\varepsilon_0}} = \sqrt{\frac{4\pi \cdot 10^{-7} \frac{H}{m}}{8.854 \cdot 10^{-12} \frac{F}{m}}} \approx 377\Omega$$

(3.1-7)

For a perfect dielectric medium the characteristic impedance is given by

$$Z_0 = \sqrt{\frac{\mu_0}{\varepsilon_0\varepsilon_r}} \approx \frac{377}{\sqrt{\varepsilon_r}}\Omega$$

(3.1-8)

3.1.2 Modeling transmission lines

Calculating transmission line impedance on a PCB is not an easy thing. It means solving Maxwell's equations for this particular structure. There are several approximations that exist but I recommend to use a 2D- or 3D-FieldSolver like Polar Instrument's Si8000m (http://www.polarinstruments.com/) . It is more precise than any approximation especially for differential striplines or microstrips.
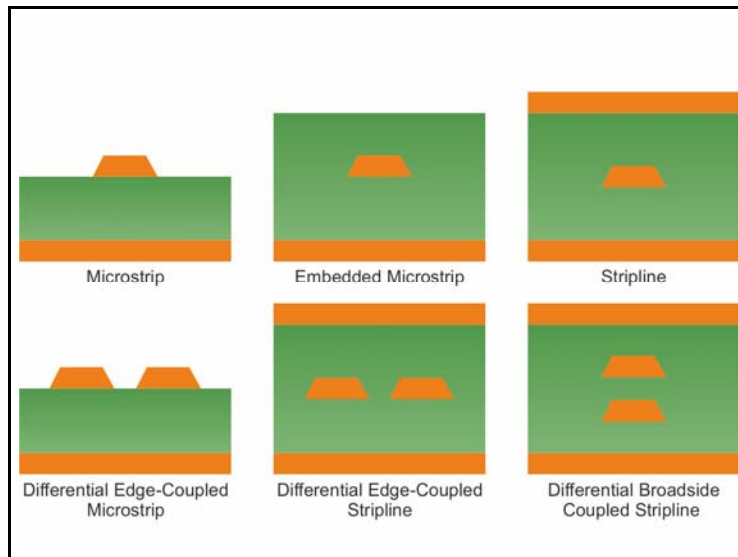
Figure 27: Types of Microstrips and Striplines

Figure 27 shows the common types of transmission lines on PCBs. A trace that re-
fers to one ground plane is called a Microstrip or Embedded Microstrip if embedded
in the dielectric. A trace that is encapsulated between two ground planes is called a
strip line. A differential signal can be transported with an Edge-Coupled Differential
Microstrip (can also be embedded), an Edge-Coupled Differential Stripline or a
Broadside Coupled Differential Stripline.

Now what is so different with transmission lines? First the voltage and the current on
a transmission line if a function of both time and position.

$$V = f(s, t) \qquad (3.1\text{-}9)$$
$$I = f(s, t) \qquad (3.1\text{-}10)$$

The voltage is related to the electric field while the current is related to the magnetic
field.
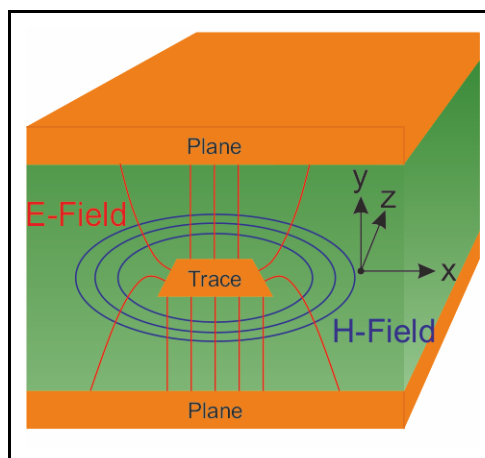
**Figure 28: Stripline with electric and
magnetic field lines**

E-Field and H-Filed form a transverse electromagnetic wave (TEM wave). E-Field and H-Field are directed transvers to the direction of propagation (the z-axis). Such waves propagate along structures composed of pairs of conductors. Since those fields have no divergence Ampère's law and Faraday's law fully describe a TEM field.

Striplines can be modeled as distributed element model.
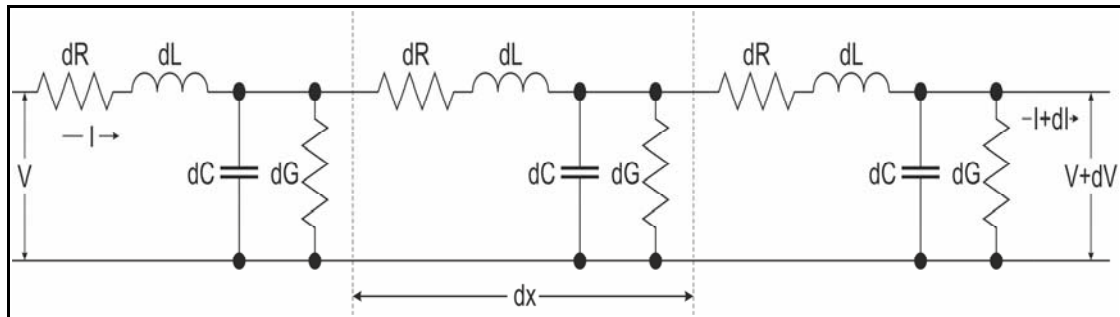
Figure 29: Distributed model of a stripline

This means that the (in this case one-dimensional) transmission line is modeled as a linear concatenation of lumped circuit elements where each element represents an infinitesimal piece of the transmission line. The model parameters are:

Model parameter	Comment	Unit
dR	Resistivity	Ω/m
dL	Distributed Inductance	L/m
dC	Distributed Capacitance	C/m
dG	Conductivity	S/m

Table 9: Parameters of a lumped element of the transmission line's distributed model

The equation describing the above model can be derived from Maxwell's equation and is called Telegrapher's Equation.

$$\frac{\delta V(x)}{\delta x} = -(dR + j\omega dL)I(x) \tag{3.1-11}$$

$$\frac{\delta I(x)}{\delta x} = -(dG + j\omega dC)V(x) \tag{3.1-12}$$

Differentiating both equations yields:

$$\frac{\delta^2 V(x)}{\delta x^2} = \gamma^2 V(x) \tag{3.1-13}$$

$$\frac{\delta^2 I(x)}{\delta x^2} = \gamma^2 I(x) \tag{3.1-14}$$

$$\gamma = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{3.1-15}$$

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3.1-16}$$

Where γ is the transmission line's complex propagation constant and Z_0 is the characteristic impedance. A solution of the above equations is:

$$V(x) = V_f e^{\gamma x} + V_r e^{-\gamma x} \qquad (3.1\text{-}17)$$
$$I(x) = I_f e^{\gamma x} - I_r e^{-\gamma x} \qquad (3.1\text{-}18)$$

Where x is the displacement from the load (negative towards source) and V_f, V_r, I_f, I_r are forward and reflected voltages and currents referring to the load (source: http://vk1od.net/transmissionline/TE/TE.htm). We now can rewrite the above equations:

$$V(x) = V_f(e^{\gamma x} + \Gamma e^{-\gamma x}) \qquad (3.1\text{-}19)$$
$$I(x) = I_f(e^{\gamma x} - \Gamma e^{-\gamma x}) \qquad (3.1\text{-}20)$$

Where Γ is the complex reflection coefficient at the load. With the load impedance Z_{load} we yield:

$$\Gamma = \frac{Z_{load} - Z_0}{Z_{load} - Z_0} \qquad (3.1\text{-}21)$$
$$\Gamma(x) = \Gamma \frac{e^{\gamma x}}{e^{-\gamma x}} \qquad (3.1\text{-}22)$$

We can now derive ρ and VSWR:

$$\rho = |\Gamma| \qquad (3.1\text{-}23)$$
$$VSWR = \frac{1 + \rho}{|1 - \rho|} \qquad (3.1\text{-}24)$$

For the quadrupole the input impedance for a transmission line of length l can now be calculated:

$$Z_{in} = Z_0 \frac{Z_{load} + Z_0 \tanh(\gamma l)}{Z_0 + Z_{load} \tanh(\gamma l)} \qquad (3.1\text{-}25)$$

Also there is the following relationship between input voltage, input current, output voltage and output current:

$$V_{in} = V_{out} \cosh(\gamma l) + I_{out} Z_0 \sinh(\gamma l) \qquad (3.1\text{-}26)$$
$$I_{in} = \frac{V_{out}}{Z_0} \cosh(\gamma l) + I_{out} \cosh(\gamma l) \qquad (3.1\text{-}27)$$

For a complete derivation see[1].

We can now distinguish between a lossless transmission line where dR and dG equals zero and a lossy transmission line where dR and/or dG do not equal zero. For a lossless transmission line therefore the above equations can be simplified.

Since the permittivity of normal materials depends on the frequency of the electric field the permittivity is complex (a material's polarization does not respond instantaneously to an electric field change and therefore introduces a phase shift).

$$\varepsilon_r = \frac{\varepsilon'}{\varepsilon_0} - j\frac{\varepsilon''}{\varepsilon_0} \qquad (3.1\text{-}28)$$

Where ε' and ε'' are the real and imaginary part of the complex permittivity. It is obvious then that

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' \qquad (3.1\text{-}29)$$

When talking about the ε_r of a PCB we mean the real part (the dielectric constant). The dielectric loss of a material can now be calculated from its complex permittivity (please remember that the parameters are a function of the frequency):

$$\tan\theta = \frac{\varepsilon''}{\varepsilon'} \qquad (3.1\text{-}30)$$

Where tan Θ equals the dissipation factor.
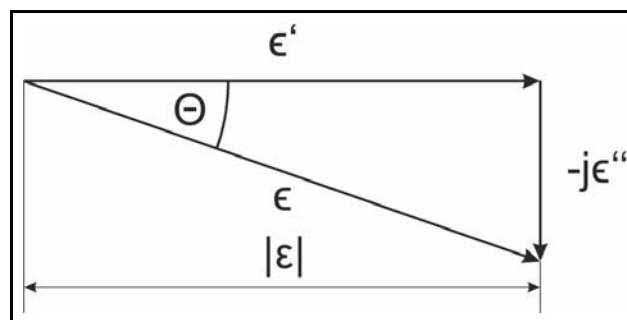
Figure 30: Dissipations factor and complex permittivity as a vector diagram

For PCB materials the dissipation factor of FR4 is causing significant attenuation in the GHz range. For 100Mbit/s and 10Mbit/s FR4 can be used. For 1GBit and especially 10GBit Ethernet a suitable high frequency material should be selected. For higher frequencies also dG depends on the frequency due to the skin effect and dR depends on the frequency as well, due to the dielectric losses.

Since the propagation velocity of electric signals on PCBs can be estimated as

$$v_{prop} = \frac{c}{\sqrt{\varepsilon_r}} \qquad (3.1\text{-}31)$$

The flight time of a signal on a PCB for a transmission line therefore can be calculated. Please be aware that vias and connectors add propagation delay as well.

3.1.3 Termination of transmission lines

Since source and load impedance and characteristic impedance of transmission lines interact, bad termination can lead to reflections [2]. For a driver injecting a signal into a transmission line a fraction of the signal is transported through the transmission line while another fraction is reflected. Since the transmitted fraction is a function of frequency we can introduce the input acceptance function A(ω):

$$A(\omega) = \frac{Z_0(\omega)}{Z_{source}(\omega) + Z_0(\omega)} \tag{3.1-32}$$

When propagating through the transmission line the signal becomes attenuated by the propagation function H(s,ω):

$$H(s, \omega) = e^{-s\sqrt{(R(\omega) + j\omega L)(j\omega C)}} \tag{3.1-33}$$

Remember that R depends on the frequency as well due to the skin effect.
At the far end of the transmission line a fraction of the attenuated signal emerges. This fraction is also a function of the frequency and is called the output transmission function:

$$T(\omega) = \frac{2Z_{load}(\omega)}{Z_{load}(\omega) + Z_0(\omega)} \tag{3.1-34}$$

The fraction of the signal that is reflected back towards the source is called the far-end reflection function:

$$R_2(\omega) = \frac{Z_{load}(\omega) - Z_0(\omega)}{Z_{load}(\omega) + Z_0(\omega)}$$

The signal now travels back towards the source, is attenuated by H(s,ω) and reflects off the source impedance. The reflection function is the near-end reflection function:

$$R_1(\omega) = \frac{Z_{source}(\omega) - Z_0(\omega)}{Z_{source}(\omega) + Z_0(\omega)} \tag{3.1-35}$$

The first signal that emerges from the transmission line can now be calculated:

$$S_0(s, \omega) = A(\omega)H(s, \omega)T(\omega) \tag{3.1-36}$$

Successive emerging signals can be calculated:

$$S_N(s, \omega) = A(\omega)H(s, \omega)[R_2(\omega)H^2(s, \omega)R_1(\omega)]^N T(\omega) \tag{3.1-37}$$

The sum of all emerging signals can be calculated from:

$$S_\infty(s, \omega) = \sum_{n=0}^{\infty} S_n(s, \omega) \tag{3.1-38}$$

A closed-form equivalent exists:

$$S_\infty(s, \omega) = \frac{A(\omega)H(s, \omega)T(\omega)}{1 - R_2(\omega)H^2(s, \omega)R_1(\omega)} \tag{3.1-39}$$

As an example we consider a stripline of 15in with a Z_0 of 50Ω and propagation delay T_P of 180ps/in. We calculate dL and dC:

$$dL = Z_0 T_P \tag{3.1-40}$$

$$dC = \frac{T_P}{Z_0} \tag{3.1-41}$$

We now model the stripline also as one lumped circuit and consider four cases for source impedance and load impedance.
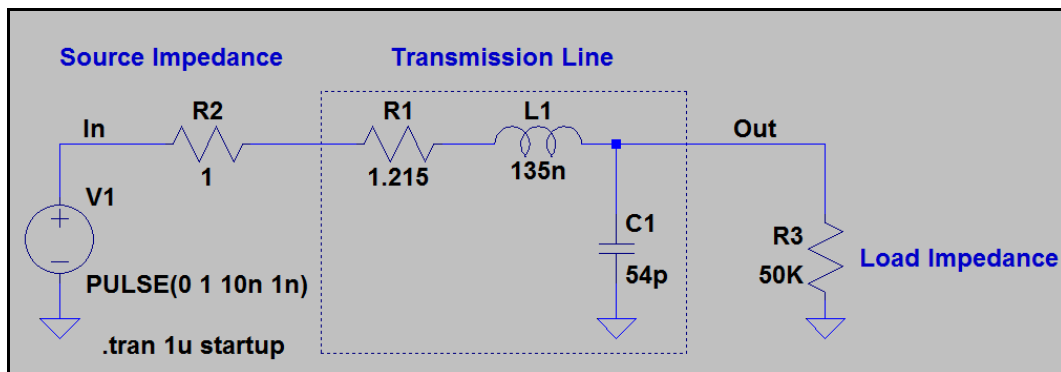
Figure 31: Lumped model of the stripline with an excitation pulse (rise time 1ns) and a load resistor.

$$R := 0.081 \frac{\Omega}{in} \qquad Z_0 := 50\Omega \qquad l := 15in \qquad T_P := 180 \frac{ps}{in}$$

$$L := Z_0 \cdot T_P \quad L = 9 \times 10^{-9} \frac{H}{in} \qquad C := \frac{T_P}{Z_0} \quad C = 3.6 \times 10^{-12} \frac{F}{in}$$

$$A(Z_{source}, \omega) := \frac{Z_0}{Z_{source} + Z_0} \qquad H(s, \omega) := e^{-s \cdot \sqrt{(R + j \cdot \omega \cdot L) \cdot j\omega \cdot C}}$$

$$R_2(Z_{load}, \omega) := \frac{Z_{load} - Z_0}{Z_{load} + Z_0} \qquad R_1(Z_{source}, \omega) := \frac{Z_{source} - Z_0}{Z_{source} + Z_0}$$

$$T(Z_{load}, \omega) := \frac{2 \cdot Z_{load}}{Z_{load} + Z_0}$$

$$S_0(Z_{source}, Z_{load}, \omega, s) := A(Z_{source}, \omega) \cdot H(s, \omega) \cdot T(Z_{load}, \omega)$$

$$f := 0Hz, 100000Hz \,..\, 1GHz$$

Figure 32: Stripline example

- Case 1: Source impedance small and load impedance high.

$$Z_{source} = 5\Omega$$
$$Z_{load} = 50K\Omega$$
$$A(100MHz) = 0.909$$
$$|H(15in, 100MHz)| = 0.988$$
$$\arg(H(15in, 100MHz) = -15°$$
$$T(100MHz) = 1.998$$
$$R_2(100MHz) = 0.998$$
$$R_1(100MHz) = -0.818$$

The amplitude at the load rises up to 1.8 times the input amplitude due to superposition of the incident and the reflected wave. The wave is reflected back and forth many times (excessive ringing).
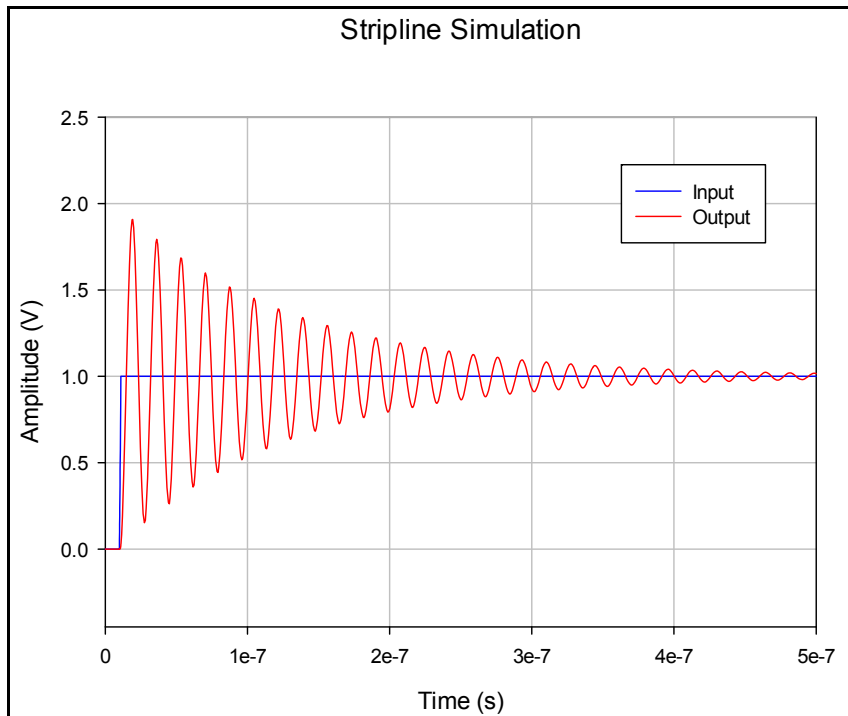
Figure 33: SPICE Stripline Simulation of case 1

- Case 2: Source impedance matched and load impedance high.

$$Z_{source} = 50\Omega$$
$$Z_{load} = 50K\Omega$$
$$A(100MHz) = 0.5$$
$$|H(15in, 100MHz)| = 0.988$$
$$\arg(H(15in, 100MHz) = -15°$$
$$T(100MHz) = 1.998$$
$$R_2(100MHz) = 0.998$$
$$R_1(100MHz) = 0$$

The amplitude at the load is round about the input amplitude due to superposition of the incident and the reflected wave where the transmission line and the source resistance for a voltage divider and therefore the incident wave is attenuated to 50% of the driver output voltage. The wave gets reflected and the reflection is absorbed in the source resistance; no further reflections occur.
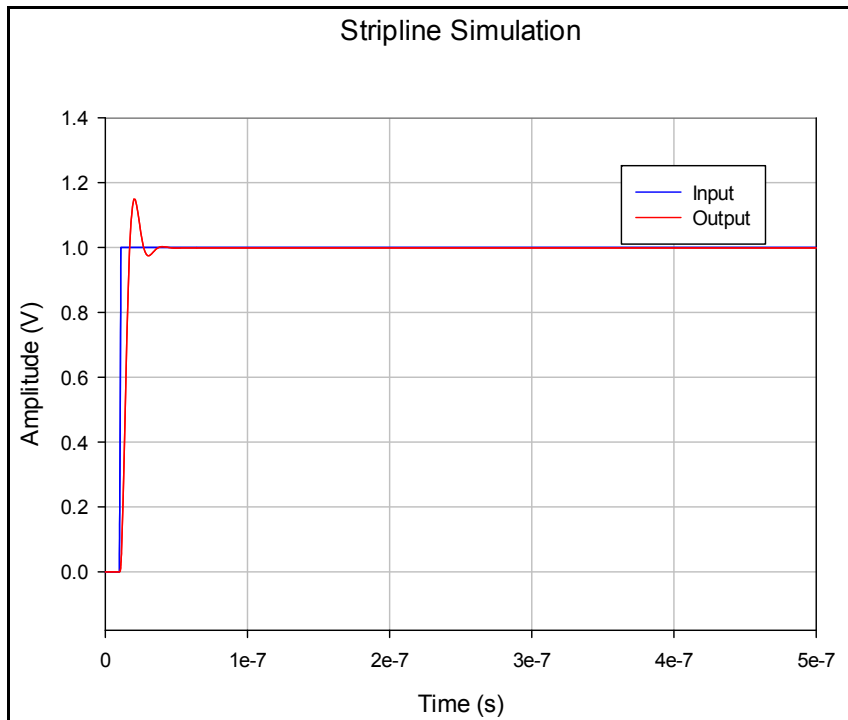
Figure 34: SPICE Stripline Simulation of case 2

- Case 3: Source impedance small and load impedance matched.

$$Z_{source} = 5\Omega$$
$$Z_{load} = 50\Omega$$
$$A(100MHz) = 0.909$$
$$|H(15in, 100MHz)| = 0.988$$
$$\arg(H(15in, 100MHz) = -15°$$
$$T(100MHz) = 1$$
$$R_2(100MHz) = 0$$
$$R_1(100MHz) = -0.818$$

The amplitude at the load is 90% of the input amplitude due to the voltage divider of the source impedance and the impedance of the stripline. Because the output is terminated, there is no reflection from the load side back to the source.
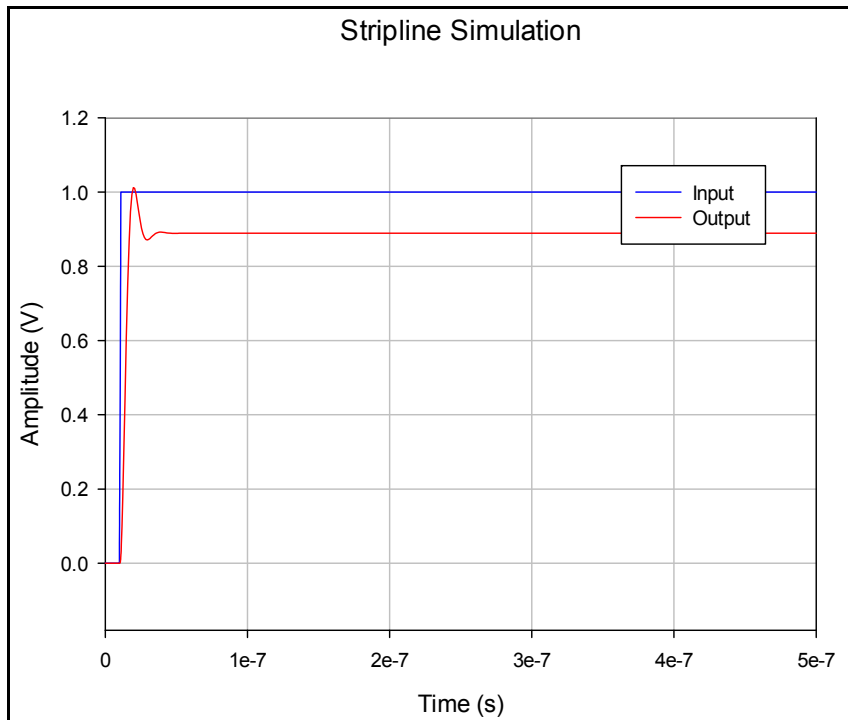
Figure 35: SPICE Stripline Simulation of case 3

- Case 4: Source impedance matched and load impedance matched.

$$Z_{source} = 5\Omega$$
$$Z_{load} = 50K\Omega$$
$$A(100MHz) = 0.5$$
$$|H(15in, 100MHz)| = 0.988$$
$$\arg(H(15in, 100MHz) = -15°$$
$$T(100MHz) = 1$$
$$R_2(100MHz) = 0$$
$$R_1(100MHz) = -0$$

The amplitude at the load is about 50% of the input amplitude due to the voltage divider formed by the source impedance and the impedance of the transmission line. There is no reflection at all.
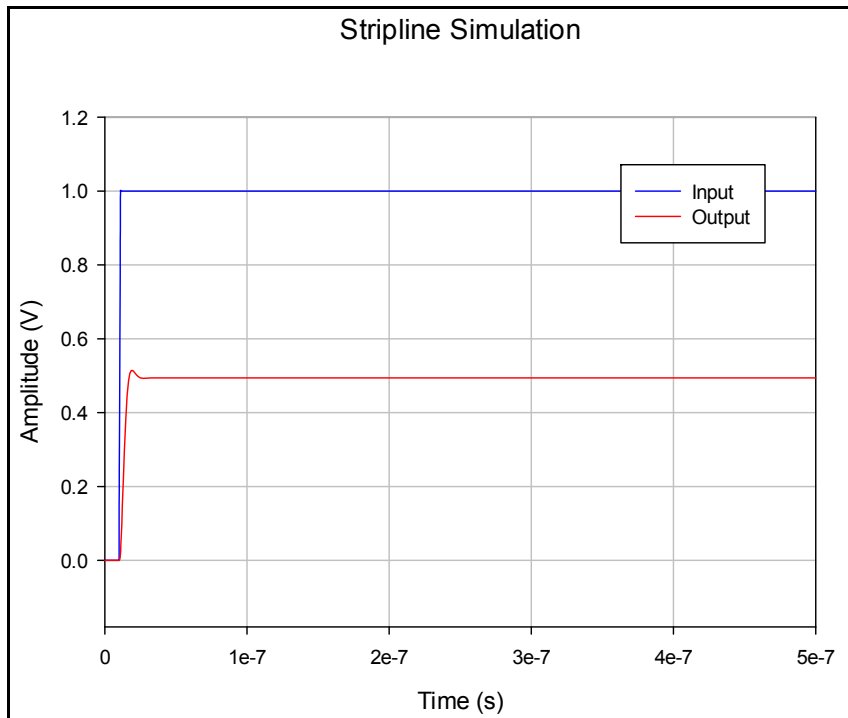
Figure 36: SPICE Stripline Simulation of case 3

We can now also calculate $S_0(\omega)$ for all 4 cases over frequency:
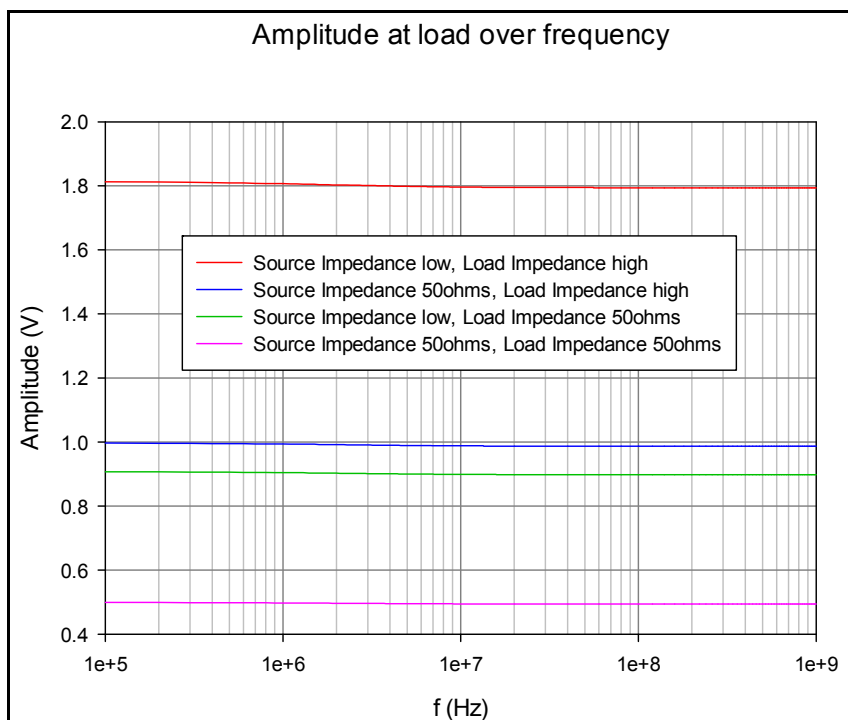
Figure 37: $S_0(\omega)$ calculated for the above 4 impedance cases

If a transmission line is that short that $H(s,\omega)$ is close to unity, we can simplify the equation for $S_\infty(s,\omega)$ [2]:

$$S_\infty(s,\omega) = \frac{A(\omega)T(\omega)}{1 - R_2(\omega)R_1(\omega)} \qquad (3.1\text{-}42)$$

$$S_\infty(s,\omega) = \frac{\dfrac{Z_0}{Z_{source} + Z_0}\dfrac{2Z_{load}}{Z_{load} + Z_0}}{1 - \dfrac{Z_{load} - Z_0}{Z_{load} + Z_0}\dfrac{Z_{source} - Z_0}{Z_{source} + Z_0}} \qquad (3.1\text{-}43)$$

$$S_\infty(s,\omega) = \frac{Z_0 2Z_{load}}{2Z_{load}Z_0 + 2Z_{source}Z_0} \qquad (3.1\text{-}44)$$

$$S_\infty(s,\omega) = \frac{Z_{load}}{Z_{load} + Z_{source}} \qquad (3.1\text{-}45)$$

The line just acts as a simple impedance divider between the source and the load impedance; it acts like a single lumped circuit element. Therefore it must be much shorter than 1/6 of the electrical length of a rising edge:

$$s \ll \frac{T_{rise}}{6\sqrt{L_{Line}C_{Line}}} \qquad (3.1\text{-}46)$$

3.1.4 The influence of Vias

If connecting capacitive load to a transmission line, the reflection from the capacitive load can be calculated [2].
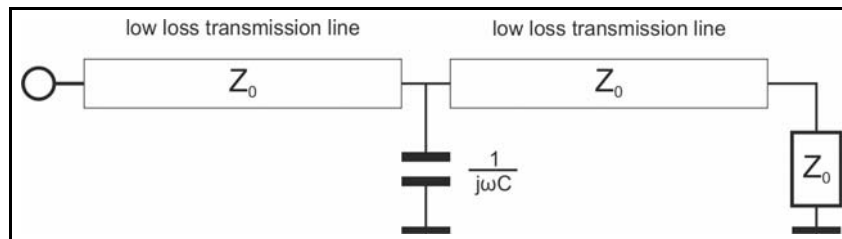
Figure 38: Transmission line with capacitive load

We assume that we deal with low loss transmission lines and that one branch of the transmission line is end terminated (there is no reflection). Its input impedance then equals to:

$$Z_0 = \sqrt{\frac{L}{C}} \qquad (3.1\text{-}47)$$

We also assume that this branch is very long and so signals reflecting off from its far end will not contribute to the reflection from the capacitive load due to their flight time.

At the capacitive load we then have a parallel combination of its impedance and Z_0. We use the following equation for the reflection:

$$R_2(\omega) = \frac{Z_{load}(\omega) - Z_0(\omega)}{Z_{load}(\omega) + Z_0(\omega)} \tag{3.1-48}$$

Substituting Z_{load} with the parallel combination of the capacitive load and Z_0 yields after simplifying:

$$R_C(\omega) = \frac{-j\omega C Z_0}{2 + j\omega C Z_0} \tag{3.1-49}$$

$$R_C(\omega) \approx \frac{-j\omega C Z_0}{2} \tag{3.1-50}$$

The latter equation looks like a differentiator (-sx). The -3dB point is reached at f=1/$CZ_0\pi$. Above this frequency the reflection is almost total.

For a signal transmitted through a capacitive load we assume again that both branches of the transmission line are long, as above, so that their effective impedance at the capacitive load can be calculated as in (xxx). We can now calculate the transmission coefficient:

$$T_C(\omega) = 1 + R_C(\omega) = \frac{1}{1 + \frac{j\omega C Z_0}{2}} \tag{3.1-51}$$

This is the equation of a first order low pass filter (1/(1+a s)) with time constant:

$$\tau = \frac{C Z_0}{2} \tag{3.1-52}$$

The 10%-90% rise time of a step response can be estimated as:

$$T_{10-90}(step\ response) = 2.2\frac{C Z_0}{2} \tag{3.1-53}$$

Now let us estimate the parasitic capacitance of a via:
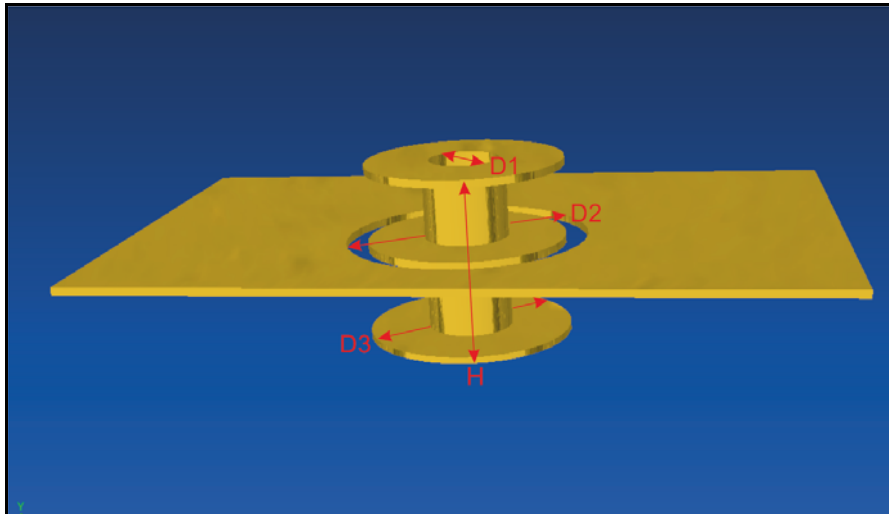
Figure 39: 3D-Model of a via (dielectric not shown)

The capacitance can only be predicted [2]. For exact calculation use a 3D-solver. The equation is:

$$C_{parasitic} = \frac{1.41\varepsilon_r H D_3}{D_2 - D_3}$$

(3.1-54)

where all measurements in inch and $C_{parasitic}$ in pF.

As an example we choose a 1.6mm PCB, a via hole diameter of 0.3mm, a via diameter of 0.6mm and a cutout diameter in the ground plane of 1.1mm. With an ε_r of 4.7 this gives a capacitance of about 0.51pF. This will effectively degrade the 10%90% rise time of a pulse by:

$$T_{10-90}(step\ response) = 2.2\frac{0.51pF \cdot 50\Omega}{2} = 28.05ps$$

(3.1-55)

So the contribution of one via is rather small.

The inductance of a via is much more important. Since a via is a small structure it behaves like a limped circuit element. The inductance can be estimated from the inner diameter and the length of the via [2]:

$$L_{parasitic} = 5.08H\left[\ln\left(\frac{4H}{D_1}\right) + 1\right]$$

(3.1-56)

Where all measurements in inch and $L_{parasitic}$ in nH.

For our example above the parasitic inductance is $L_{parasitic}$ = 1.2nH. This parasitic inductance increases the impedance of the current path to bypass capacitors and therefore degrades their effectiveness. At 100MHz the via has an Impedance of

about 0.75Ω and at 1GHz about 7.5Ω. If we have a rising edge with a T_{10-90} of 1ns the impedance is about 3.8Ω. Since a 1n ceramic capacitor has an ESR in this frequency range of below 1Ω the via together with the cap forms a 4:1 (!) voltage divider and the effectiveness of the bypass capacitor is down to ¼.

3.2   Layout and Timing

3.2.1 Calculation of timing requirements

Having discussed the theory of transmission lines we now will discuss the layout techniques to improve signal integrity and reduce EMI. First of all to have a functional device, we must guarantee that the required timing of all integrated circuit is met. I will show that at an example design with a FREESCALE processor with integrated MAC and a DAVICOM PHY using an RMII interface. Now let us check the timing of the RMII interface. Since we use a crystal oscillator to source the clock for both, the PHY and the processor we must take care of the clock timing and the impedance of the clock line. The highest timing margin – since RMII is bidirectional using only one clock – can be achieved if the clock reaches the MAC and the PHY at the same time. Therefore a PCB microstrip structure called "balanced T" is used: Place the 50MHz crystal in the middle between the MAC and the PHY.
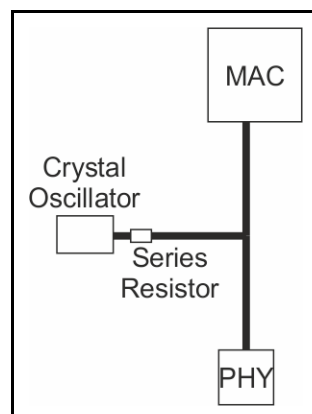
Figure 40: Balanced T structure

Put a series resistor for source impedance matching directly at the oscillator and route towards the MAC and the PHY as close as possible. Then route to the PHY and the MAC in a T-like structure keeping both traces as short as possible and of equal length. This guarantees that the clock arrives at the MAC and the PHY at the same time.

In order to meet the timing requirements all data and control lines that refers to the 50MHz clock should be not shorter than the clock line. No let us assume that the total clock trace length to the PHY and to the MAC is 2''. We now try to match all traces that references to the clock to 2'' as well. The timing requirements for TXD[1:0] referenced to the clock is shown in Figure 41. The maximum clock-to-output time for the MAC is 15ns. Since the minimum setup time for the PHY is 4ns we have a margin of

1ns for signal rise and fall time as well as the flight time on the PCB trace. For a 2''
transmission line on FR4 the propagation delay is about 180ps/in therefore for a 2''
trace the propagation delay is about 0.36ns. So even a 3'' data trace would keep the
setup timing within its margins. The minimum hold time of the PHY is 2ns and the
minimum clock-to-output time for the MAC is 4ns. The margin for the hold time there-
for is 2ns and each inch of data trace would even increase the margin. Since the
margin for the hold time is larger than for the setup time one could think about mak-
ing the clock traces longer than the data traces.
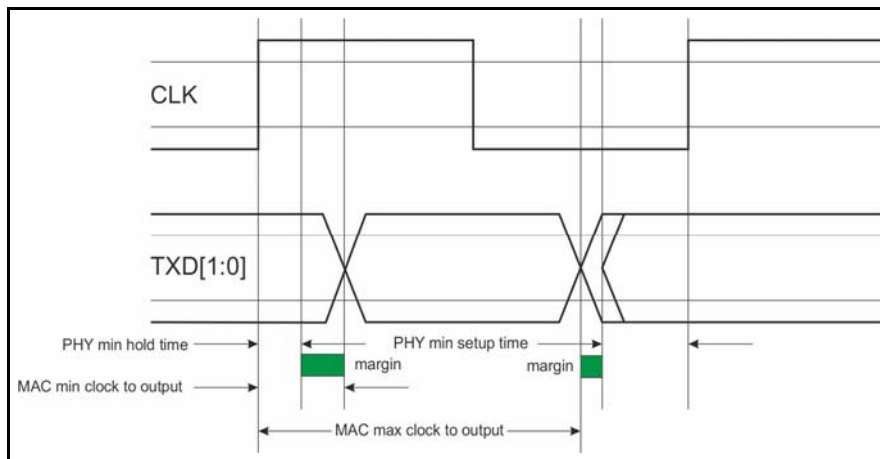
Figure 41: Timing requirements for TXD[1:0]

Unfortunately the clock-to-output timing of the RMII interface of the selected DAVI-
COM PHY (DM9161C) is not specified in its datasheet.

3.2.2 Layouting traces on the PCB

Since we need length matching for signals use a layout system which supports that.
My layout system lets me adjust the length matching parameters and semi-
automatically lets me length match a trace with a meander-like structure.
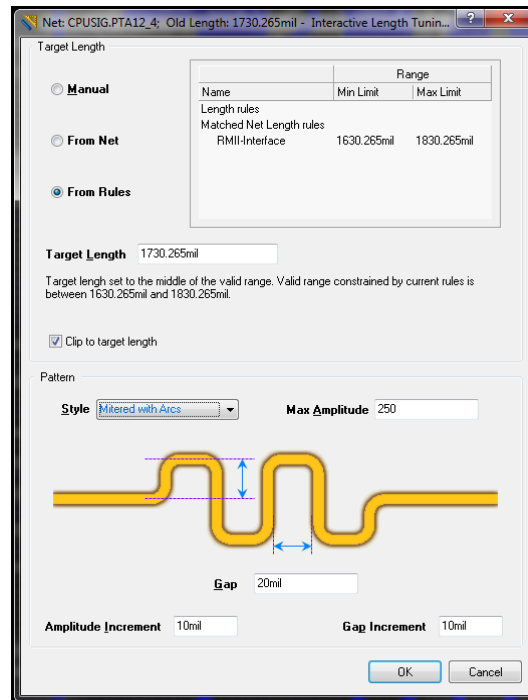
**Figure 42: Adjustment of length matching pa-
rameters in layout system**

You should use arcs for mitering since rectangular mitering alters the cross section of
the trace and therefore will introduce impedance "bumps". For semi-automatic length
matching the system tries to match to a target length and shows a bargraph that fol-
lows a length-matching-rule.

**Figure 43: Semi-automatic length matching of a PCB
trace.**

The length matching rule must be adjusted to the required timing margin from the
timing calculation above. My system allows to define net classes for signals and I can
then define a rule for such a net class. The following figure shows a length-matching-
rule with a tolerance of 100mil for a net class "RMII-Interface".
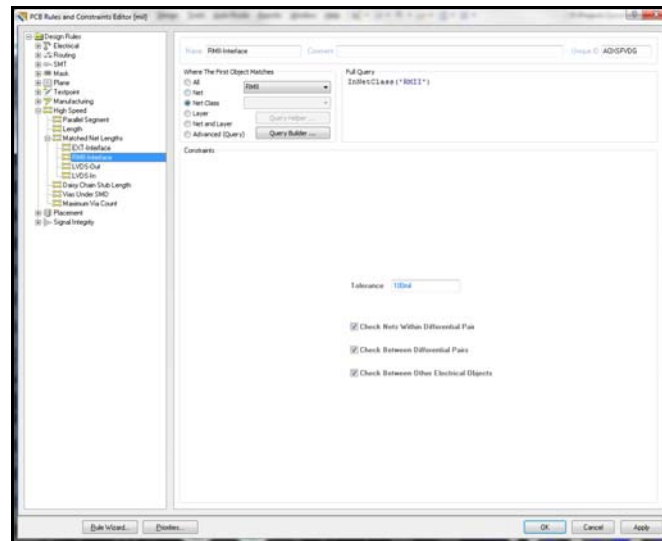
Figure 44: Length matching rule for the RMII interface.

After length matching the traces in the layout check carefully for crosstalk possibilities. Avoid paralleling of traces over a long distance and also keep other traces away from clock traces at least 3 times of the trace width. Also try to keep the number of vias in a trace low since vias are impedance discontinuities and introduce an additional delay.
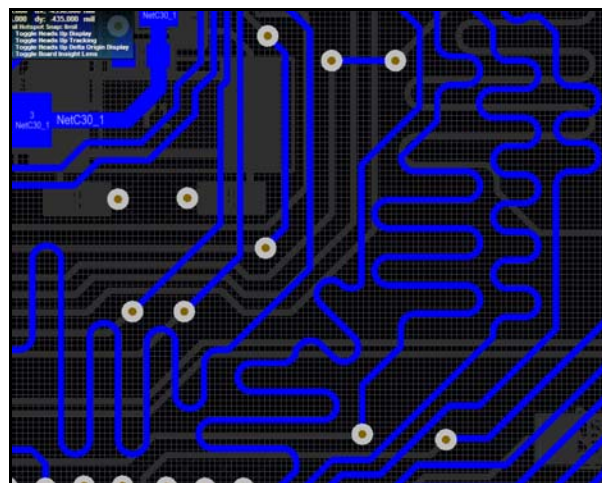
Figure 45: Layout on one Layer after length matching.

For the differential TX+/- and RX+/- pairs between PHY and magnetics you must also define routing rules.
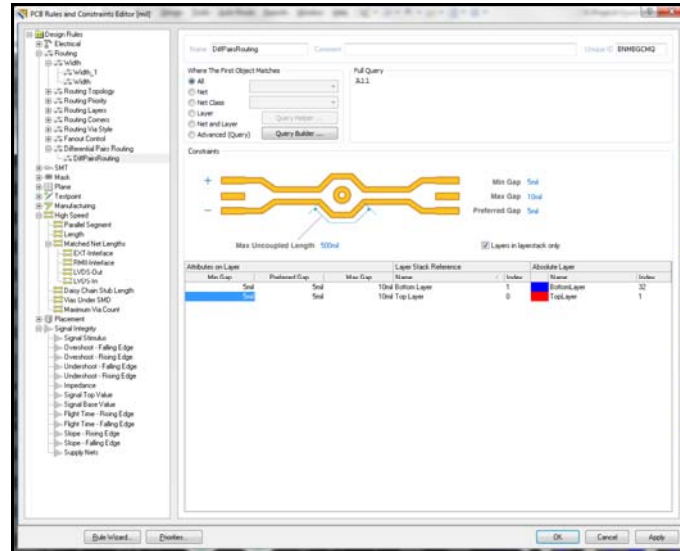
Figure 46: Routing rule for differential pair routing.

You should keep the uncoupled length as small as possible and obey the gap rule.

A differential pair also needs to match within the pair. The difference in length between both traces must be kept as small as possible. If bending the differential pair in one direction the outer traces become elongated. So for compensation you should bend the differential pair into the opposite direction.
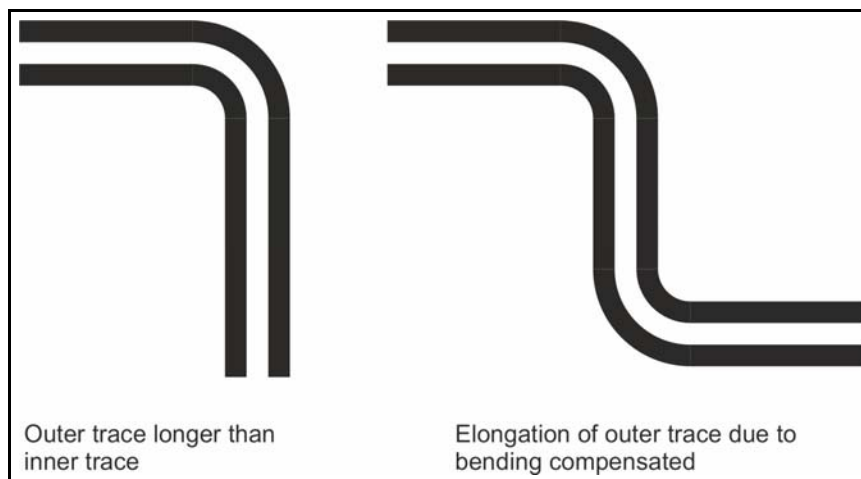
Figure 47: Compensation of length mismatching in differential pairs

3.2.3 Layer stack, VCC and GND planes in the layout

You should use at least a 4-Layer design since a GND-plane is mandatory. Also the design should be impedance-controlled and the required dimensions should be calculated by means of a 2-D or 3-D solver. This can be done in most cases by the PCB manufacturer.
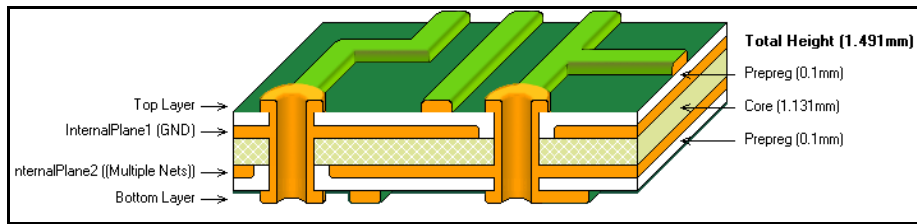
Figure 48: Typical 4-Layer Stack of an impedance controlled design
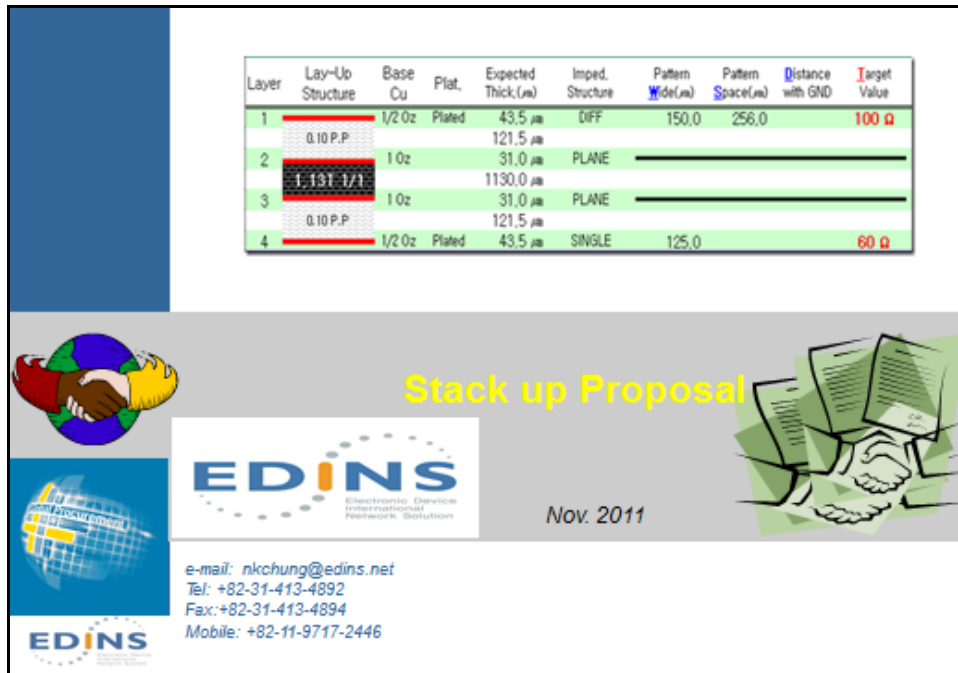
Figure 49: Layer stack calculation provided by the PCB manufacturer

The impedance from the power or ground plane to the supply pads of a device should be kept as low as possible. For a low impedance supply bypassing, use a combination of different capacitors like 100n and 1n.
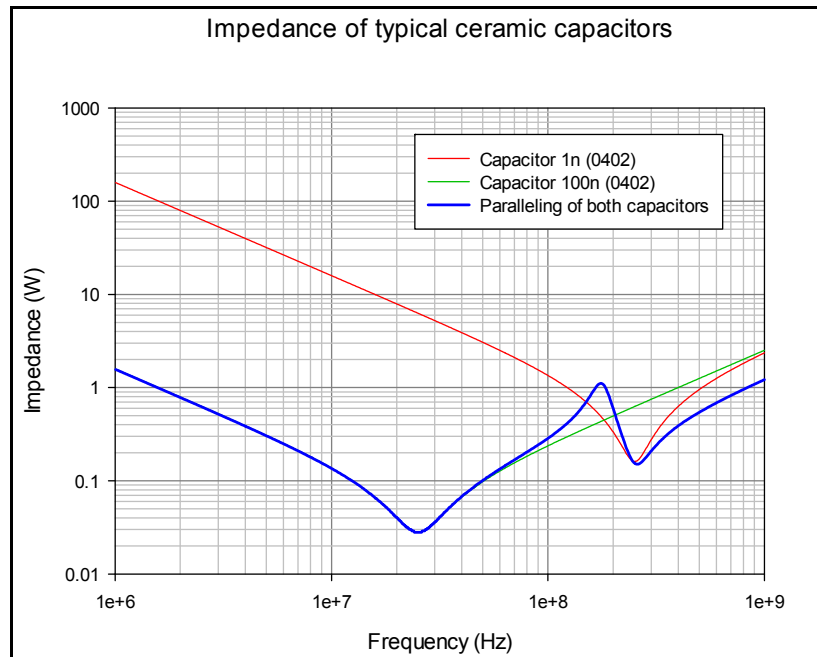
Figure 50: Paralleling of bypass capacitors of different value gives a low impedance over the whole frequency range

To decrease the influence of the via inductance use two or three vias to connect the bypass capacitors to the plane instead of one. This is also true for large bulk capacitors, sincethe vias must be capable to carry the current there. Small capacitors must be placed very close to the supply pad to keep the high frequency impedance low. Larger capacitors or bulk capacitors can be placed further away.
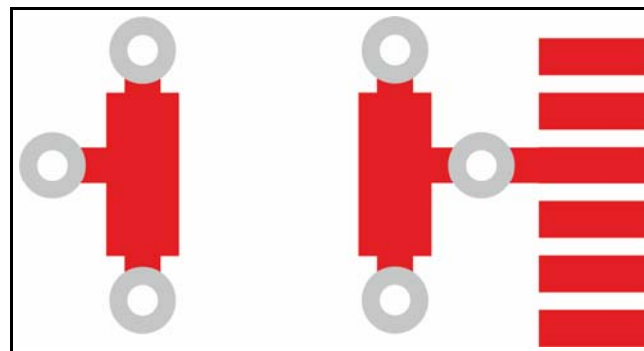
Figure 51: Routing of a bypass capacitor

Do not use Z5U dielectric material capacitors since they have worse aging, temperature coefficient and capacity loss due to DC biasing, use X7R or X5R.

Since most PHYs have an analog and a digital domain you should avoid current passing from the digital domain into the analog domain. This can be done by slotting the ground plane but leave a broad tab as connection between digital and analog ground plane at one point. Also a connection between chassis ground and analog ground may be beneficial (or not! You have to check that in the EMI lab). If using a capacitive coupling between analog ground and chassis ground, be aware that you need several capacitors of different capacity to guarantee a low impedance connec-

tion over the whole frequency range. This depends on your hardware, as well as on the enclosure of the device.
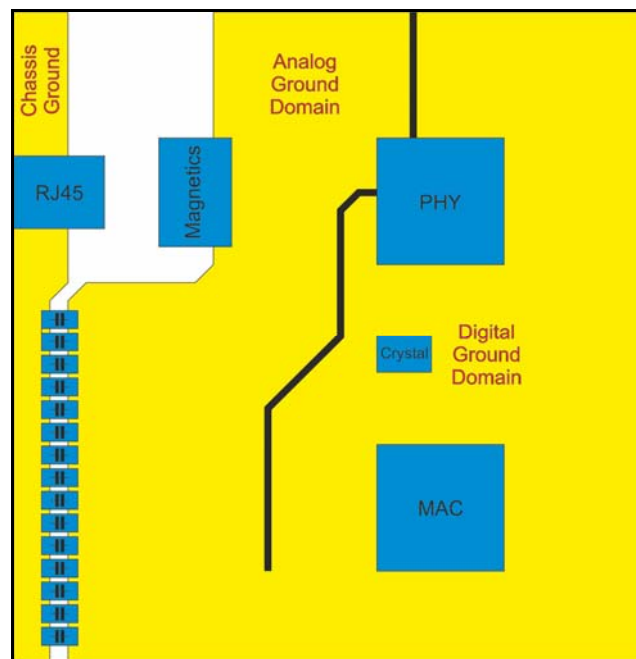
Figure 52: Ground plane design in a typical Ethernet application

3.2.4 Where to put the termination resistors

Ethernet uses parallel termination. That means that the termination network has to be placed close to the RX pins of the PHY. Normally two 49R9 resistors which are connected together are used. The midpoint (the connection between the resistors) is then ac-terminated to GND by means of a 100n capacitor. This terminates both lines independently. If you would use only a single 100Ω resistor between both lines and if you have a skew between the RX+ and the RX- signal then the 100Ω resistor would create two artifacts during the skew interval (crosstalk from RX+ to RX- and vice versa; see Dr. Howard Johnson:
http://www.sigcon.com/Pubs/edn/DifferentialTermination.htm). Since many PHYs use a differential current source as transmitter the transmit lines need 50Ω pullups to VCC. Place those resistors as close as possible to the TX pins of the PHY. Placing all termination networks close to the PHY helps to reduce the return loss.

3.2.5 Miscellaneous

DAVICOM PHYs use an internal bandgap voltage reference that needs an external resistor. This resistor must be placed close to the pads of the PHY. Since this resistor adjusts the internal bandgap, no high speed signal should be placed close to it nor should any high speed trace run under it. The resistor should be placed on the analog ground plane.

The crystal oscillator's frequency stability is critical. It should be 50ppm or better (as required by the specification). Placement of the oscillator for an RMII interface device has been discussed earlier. DAVICOM suggests a placement close to the PHA but due to the timing of the RMII interface the clock must reach the PHY and the MAC at the same time and so I recommend a placement in the middle between MAC and PHY.

Plane cutouts and routing limitations due to compliance with safety requirements has been discussed earlier.

Place the connector close to the magnetics. Since you do not have a ground plane there, you cannot keep the impedance requirement. The distance between MAC and PHY is not that critical and depends on the quality of your striplines or microstrips, as well as on the timing requirements of the interface as discussed above.

3.3   Some words about the magnetics

The magnetics consist of the Ethernet isolation transformer and a common mode choke for EMI suppression. Let us have a closer look at the theory of a transformer and its real model [6].

3.3.1 Inductance in a transformer

From Faraday's Law we can write:

$$\varepsilon_{21} = -N_2 \frac{d}{dt}\phi_{21} = \frac{d}{dt}\iint \vec{B}_1 d\vec{A}_2 \qquad (3.3\text{-}1)$$

$$\varepsilon_{12} = -N_1 \frac{d}{dt}\phi_{12} = \frac{d}{dt}\iint \vec{B}_2 d\vec{A}_1 \qquad (3.3\text{-}2)$$

The derivative of the magnetic flux is proportional to the derivative of the current

$$N_2 \frac{d}{dt}\phi_{21} = M_{21}\frac{d}{dt}I_1 \qquad (3.3\text{-}3)$$

$$N_1 \frac{d}{dt}\phi_{12} = M_{12}\frac{d}{dt}I_2 \qquad (3.3\text{-}4)$$

where M_{21} and M_{12} is known as Mutual Inductance. Therefore:

$$M_{21} = \frac{N_2 \phi_{21}}{I_1} \qquad (3.3\text{-}5)$$

$$M_{12} = \frac{N_1 \phi_{12}}{I_2} \qquad (3.3\text{-}6)$$

The Reciprocity Theorem let us show the equality of both terms:

$$\langle a, b \rangle = \langle b, a \rangle, where \; \langle a, b \rangle = \iiint [E^a(J^b - H^a M^b)]dv \qquad (3.3\text{-}7)$$

$$M_{12} = M_{21} = M \qquad (3.3\text{-}8)$$

Self inductance (back emf):

The self induced emf is:

$$\varepsilon_L = -N\frac{d}{dt}\phi_B \qquad (3.3\text{-}9)$$

$$\varepsilon_L = -N\frac{d}{dt}\iint B dA \qquad (3.3\text{-}10)$$

The self inductance now is:

$$\varepsilon_L = -L\frac{d}{dt}I \qquad (3.3\text{-}11)$$

$$L = \frac{\varepsilon_L}{-\frac{d}{dt}I} \qquad (3.3\text{-}12)$$

$$L = \frac{-N\frac{d}{dt}\phi_B}{-\frac{d}{dt}I} \qquad (3.3\text{-}13)$$

$$L = \frac{N\phi_B}{I} \qquad (3.3\text{-}14)$$

Self inductance of a toroid:

We consider a toroid with radius r and cross section a x b.

According to Ampere's law:

$$\int \vec{B}ds = \int B ds = B\int ds = B(2\pi r) = \mu_0 NI \qquad (3.3\text{-}15)$$

$$B = \frac{\mu_0 NI}{2\pi r} \qquad (3.3\text{-}16)$$

The flux now is:

$$\phi_B = \iint \vec{B}dA = \int_{r-\frac{a}{2}}^{r+\frac{a}{2}} \frac{\mu_0 NI}{2\pi r} b dr \qquad (3.3\text{-}17)$$

$$\phi_B = \frac{\mu_0 NI}{2\pi r} b \cdot \ln\left(\frac{r + \frac{a}{2}}{r - \frac{a}{2}}\right) \tag{3.3-18}$$

$$L = \frac{N\phi_B}{I} = \frac{\mu_0 N^2 b}{2\pi} \cdot \ln\left(\frac{r + \frac{a}{2}}{r - \frac{a}{2}}\right) \tag{3.3-19}$$

If r << a this can be approximated:

$$l\,n\left(\frac{r + \frac{a}{2}}{r - \frac{a}{2}}\right) = \frac{r + \frac{a}{2} - \left(r - \frac{a}{2}\right)}{r - \frac{a}{2}} = \frac{a}{r - \frac{a}{2}} \tag{3.3-20}$$

$$L = \frac{\mu_0 N^2 b}{2\pi} \cdot \frac{a}{r - \frac{a}{2}} = \frac{\mu_0 N^2 A}{2\pi \left(r - \frac{a}{2}\right)} = \frac{\mu_0 N^2 A}{l} \tag{3.3-21}$$

$$l = 2\pi \left(r - \frac{a}{2}\right) \tag{3.3-22}$$

We can now recalculate the Mutual Inductance from the Self Inductance of both coils:

$$\phi_{21} = BA = \frac{\mu_0 N_1 I}{l} A \tag{3.3-23}$$

$$M = \frac{N_2 \phi_{21}}{I_1} = \frac{\mu_0 N_1 N_2}{l} A \tag{3.3-24}$$

$$L_1 = \frac{N_1 \phi_{11}}{I_1} = \frac{\mu_0 N_1{}^2}{l} A \tag{3.3-25}$$

$$L_2 = \frac{N_2 \phi_{22}}{I_2} = \frac{\mu_0 N_2{}^2}{l} A \tag{3.3-26}$$

$$L_1 L_2 = \frac{\mu_0 N_1{}^2}{l} A \cdot \frac{\mu_0 N_2{}^2}{l} A = \frac{\mu_0{}^2 N_1{}^2 N_2{}^2 A^2}{l^2} \tag{3.3-27}$$

$$\sqrt{L_1 L_2} = \frac{\mu_0 N_1 N_2 A}{l} = M \tag{3.3-28}$$

Since the core material is not air we substitute:

$$\mu_0 = \mu_0 \mu_r \tag{3.3-29}$$

Now the emf on both sides can be calculated as sum of self inductance and mutual inductance:

$$emf_1 = L_1 \frac{d}{dt} I_1 + M \frac{d}{dt} I_2 \tag{3.3-30}$$

$$emf_2 = L_2 \frac{d}{dt} I_2 + M \frac{d}{dt} I_1 \tag{3.3-31}$$

$$emf_1 = \frac{\mu_0 N_1{}^2 A}{l} + \frac{\mu_0 N_1 N_2 A}{l} \tag{3.3-32}$$

$$emf_2 = \frac{\mu_0 N_2{}^2 A}{l} + \frac{\mu_0 N_1 N_2 A}{l} \tag{3.3-33}$$

$$emf_1 = \frac{\mu_0 A \left(N_1{}^2 + N_1 N_2\right)}{l} = \frac{\mu_0 A \left(N_1{}^2 + N_1{}^2 n\right)}{l} \tag{3.3-34}$$

$$emf_2 = \frac{\mu_0 A \left(N_2{}^2 + N_1 N_2\right)}{l} = \frac{\mu_0 A \left(\left(N_1 \frac{1}{n}\right)^2 + N_2{}^2 \frac{1}{n}\right)}{l} \tag{3.3-35}$$

$$emf_1 = \frac{\mu_0 A N_1{}^2}{l}(n+1) \tag{3.3-36}$$

$$emf_2 = \frac{\mu_0 A N_1{}^2}{l} n(n+1) \tag{3.3-37}$$

$$\frac{emf_1}{emf_2} = \frac{n+1}{n(n+1)} = \frac{1}{n} \tag{3.3-38}$$

Since:

$$P_1 = P_2 \tag{3.3-39}$$

Also:

$$\frac{I_2}{I_1} = \frac{1}{n} \tag{3.3-40}$$

For the impedance we can now calculate:

$$P = \frac{emf_1{}^2}{Z_1} = \frac{emf_2{}^2}{Z_2} \tag{3.3-41}$$

$$\frac{Z_1}{Z_2} = \frac{emf_1{}^2}{emf_2{}^2} = \frac{1}{n^2} \tag{3.3-42}$$

Since we do not have an ideal coupling of the two coils (e.g. there are magnetic flux lines that do not pass the cross section of both coils and they form the leakage inductance), we must rewrite the mutual inductance:

$$M = k\sqrt{L_1 L_2} \qquad\qquad (3.3\text{-}43)$$

Where k is the coupling factor and:

$$0 \le k \le 1 \qquad\qquad (3.3\text{-}44)$$

3.3.2 Modeling a real world transformer

The real world model of a transformer looks different than an ideal transformer. A real transformer has several parasitic properties:

- Not all field lines of one winding pass through the other winding, thus contributing to the mutual inductance. This leakage inductance acts like an uncoupled inductor.
- The close proximity of the windings leads to capacitive coupling called interwinding capacitance.
- The distributed interwinding capacitance models the capacitive coupling between consecutive windings
- The magnetizing inductance accounts for the finite permeability of the magnetic core
- The winding resistance models the dc resistance of the winding
- The core losses are modeled by a resistor. This is only valid for a specific frequency
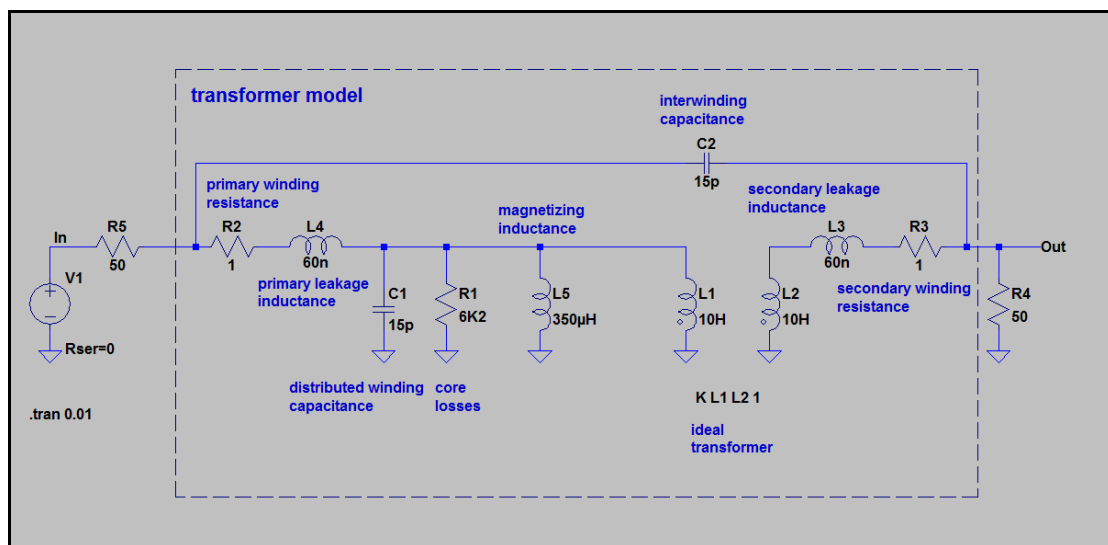
Figure 53: Real world transformer model with typical values for a 10/100Mbit Ethernet transformer

The above spice model can be used to simulate the answer to a square wave with a frequency of 31.25MHz.
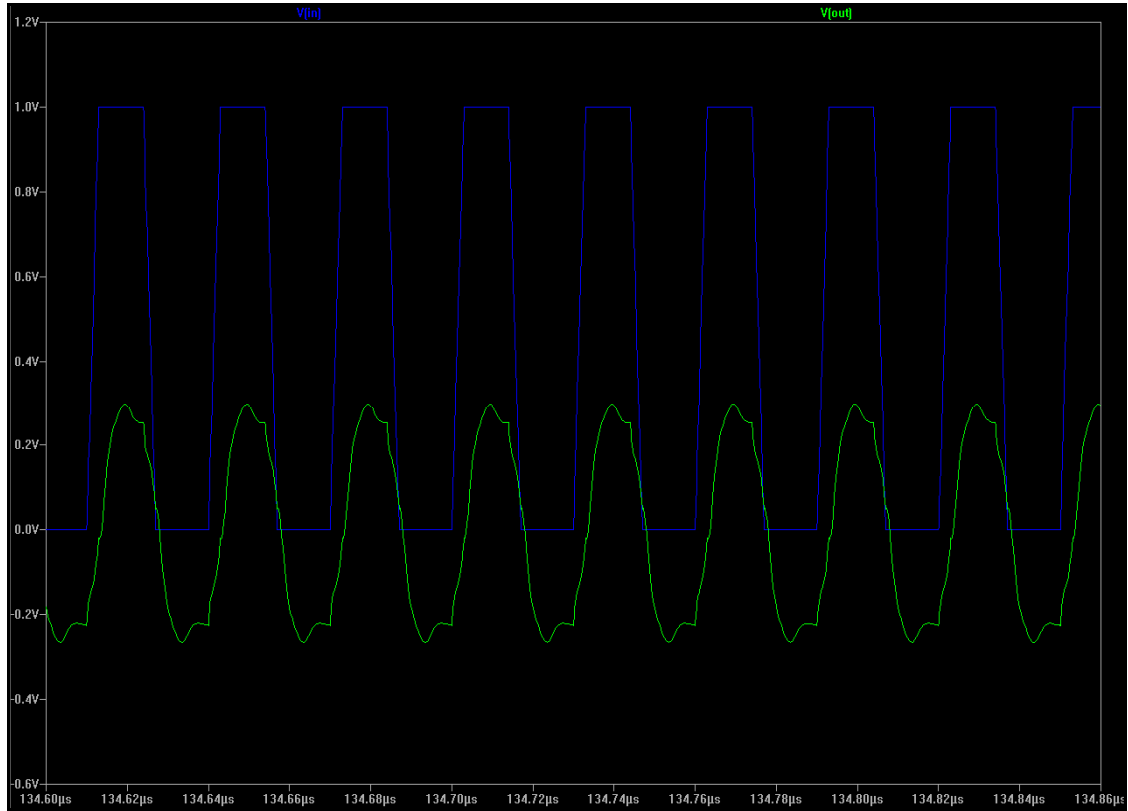
Figure 54: Simulation of the answer to a 31.25MHz square wave input into the above transformer model.

Also the voltage droop of the transformer can be simulated.

Figure 55: Simulation of voltage droop to a step function.

3.4   Measuring and Measurement Equipment

3.4.1 Measurement equipment

Compliance testing for 10/100Mbit Ethernet does require special equipment. If a compliance test is required you can use special software together with a good oscilloscope and a differential active probe. The application software is available from the oscilloscope vendors such as Tektronix, Agilent and LeCroy, see:

http://www.tek.com/sites/tek.com/files/media/media/resources/61W_26144_4.pdf

http://cp.literature.agilent.com/litweb/pdf/5989-1527EN.pdf

http://www.lecroy.com/serialdata/serialdatastandard.aspx?standardid=171&capid=105&mid=520

For signal integrity measurements on the MII or RMII interface you need a good 1GHz-Scope and an active (low capacitance) probe. A normal probe is not sufficient! You should also avoid long ground wires, since their inductance may introduce ringing and the circuit can induce noise in the magnetic loop antenna formed by the ground wire. The capacitance of the probe deteriorates the rise time of rectangular signals, since the device under test must charge that capacitance through its source impedance. An active probe has a typical capacitive load of about 0.5pF whereas typical passive probe has a typical capacitive load of about 10pF. Also the bandwidth

of the probe has an influence on the form of the signal, since it attenuates frequency components above the bandwidth (-3dB-point) with 6dB/octave.
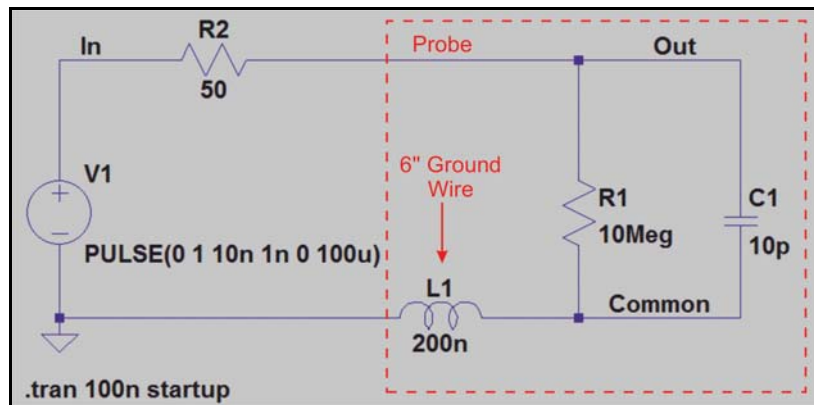
Figure 56: Typical passive probe with a 6" ground wire connected to a 50Ω source.
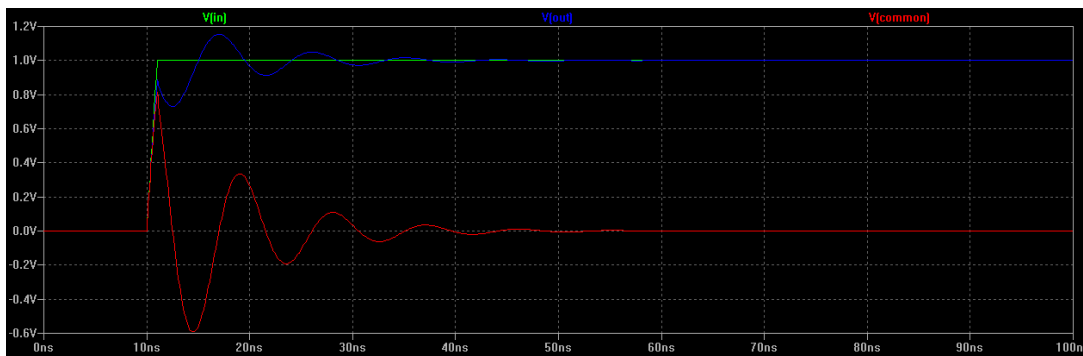
Figure 57: Response of the above circuit to a rising edge with a rise time of 1ns.

In the following paragraphs I will show some typical probes and explain how to use them.

Figure 58: Typical active single ended probe (TAP1500 from Tektronix Inc.)

Figure 58 shows a typical single ended active FET probe with an input capacitance smaller than 1pF and a bandwidth greater than 1.5GHz.These probes can be dam-

aged by excessive voltage amplitudes (greater than ±15V) and do not allow AC coupling. When using the probe try to keep the ground connection as short as possible.
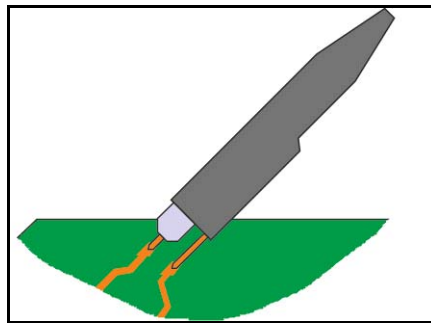
Figure 59: Applying a probe to a PCB with shortest possible ground connection.

If measuring differential signals use a differential probe. Do not use two single ended probes and internal scope math to subtract the two signals. The CMRR of such a measurement for high frequency signals is much worse than using a real differential probe.

Figure 60: Typical differential active probes (TDP1500 and TDP3500 from Tektronix Inc.)

Please obey the maximum common mode input range when using differential probes.

For specialized measurements you maybe have to directly attach the DUT to the scope. You then have to use proper HF connectors like SMA and the receptacle has to be design in your PCB. Also check for proper impedance matching.

3.4.2 Some words about jitter

Jitter measurement is not an easy thing to do. First we must understand the mathematical background. First we will define what jitter is: Jitter is the short-term variation of the periodicity of a digital periodic signal. We can define:

- Periodic jitter: variation of the period of consecutive clock cycles over time
- Cycle-to-Cycle Jitter: variation of the period difference of two consecutive clock cycles over time

To qualify the Jitter we need to use a stochastic classification using mean and standard deviation. Also we need to define the root mean square (RMS):

The root mean square or quadratic mean is defined as:

$$RMS = \sqrt{\frac{1}{n}\sum_{i=1}^{n} x_i{}^2} \qquad (3.4\text{-}1)$$

Since the standard deviation is defined as the square root of the sum of squares of errors:

$$s = \sqrt{\frac{1}{n}\sum_{i=1}^{n} (x_i - \bar{x})^2} \qquad (3.4\text{-}2)$$

Where $\bar{x}$ is the mean and s is the standard deviation of a random sample representing the underlying stochastic process with mean μ and standard deviation σ.

It is obvious that if the mean value equals zero the standard deviation equals the RMS value.

Now we have to define the distribution of these errors. If we assume that the distribution is Gaussian we can define the normal distribution:

$$f(x) = \frac{1}{\sqrt{2\pi}\sigma} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \qquad (3.4\text{-}3)$$

Assuming that μ = 0 and σ^2 = 1 we can define the standard normal distribution which is a probability density function

$$f(x) = \frac{1}{\sqrt{2\pi}} e^{-\frac{x^2}{2}} \qquad (3.4\text{-}4)$$

and the cumulative standard normal distribution which is a probability function

$$F(x) = \int_{k=0}^{x} \frac{1}{\sqrt{2\pi}} e^{-\frac{k^2}{2}} \qquad (3.4\text{-}5)$$

Fig shows the graph of (3.4-4) and (3.4-5):
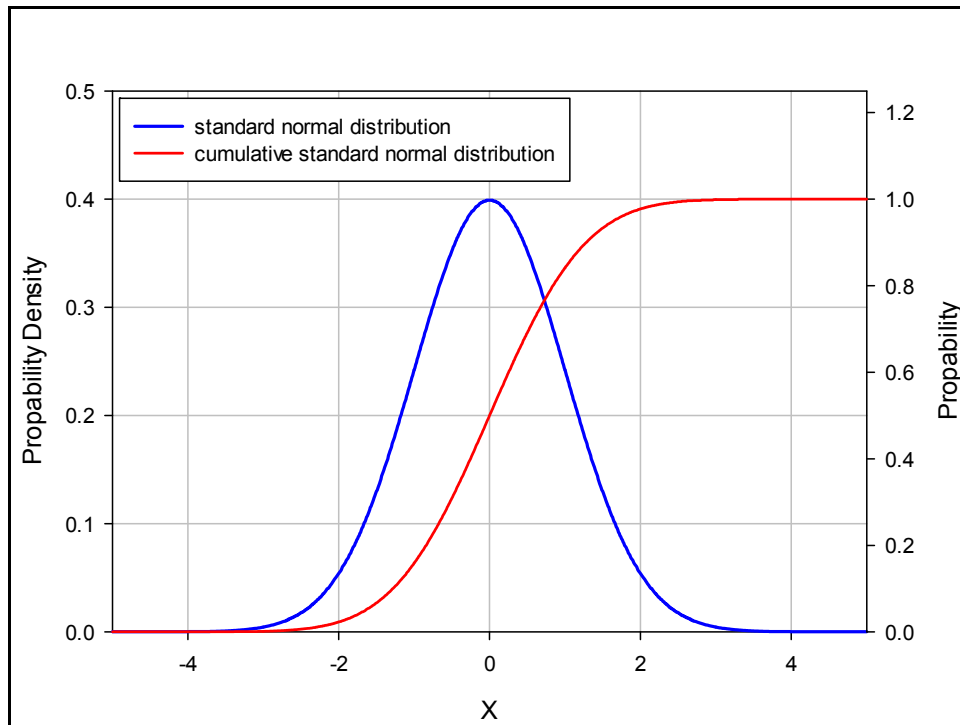
Figure 61: Plot of the normal probability density and cumulative normal probability density function

Now since we assume that jitter follows a Gaussian distribution, we can put our consecutive jitter measurements into a histogram and from a normal distribution fitted into that histogram we can predict the probability for the jitter to fall into a specified range. The probability can be calculated by integrating the normal distribution from –x to x and therefore it's the area under the normal distribution.
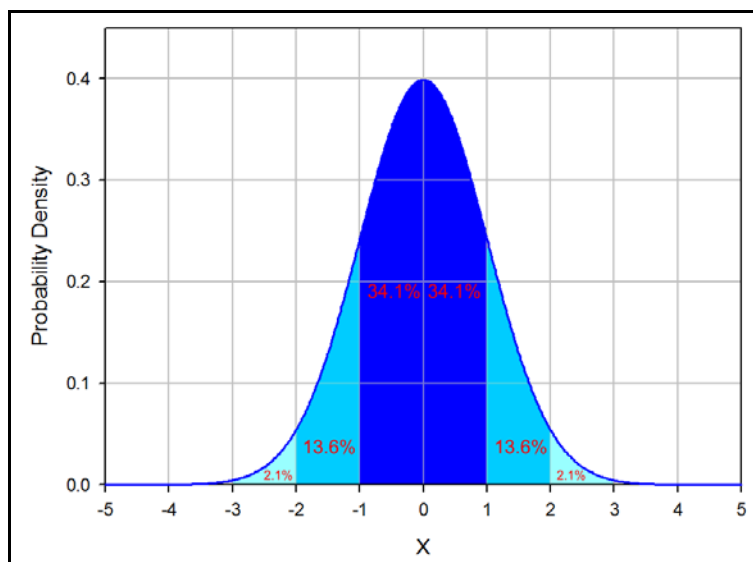
Figure 62: Probability area below the normal distribution curve

If we integrate from -1 to 1 which - since $\sigma^2 = 1$ - means from -σ to σ we can show that about 68% of all values drawn from a normal distribution are within that interval.

Therefore for every interval [-m·σ,m·σ] we can calculate the probability P of being between the limits of that interval and of being outside (which is the error probability α = 1 – P).
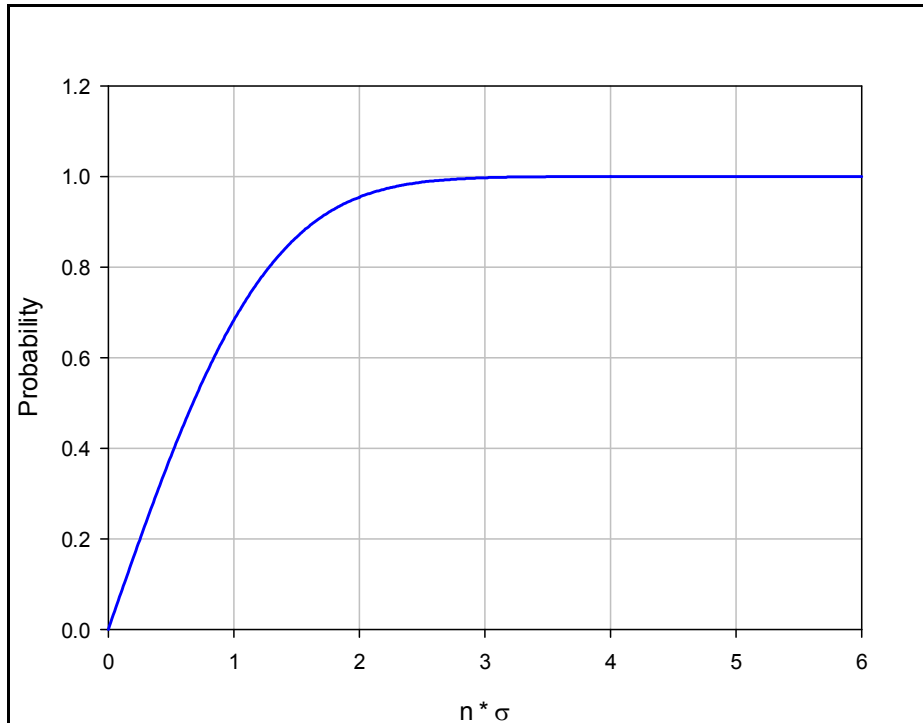
Figure 63: Probability as a function of n · σ
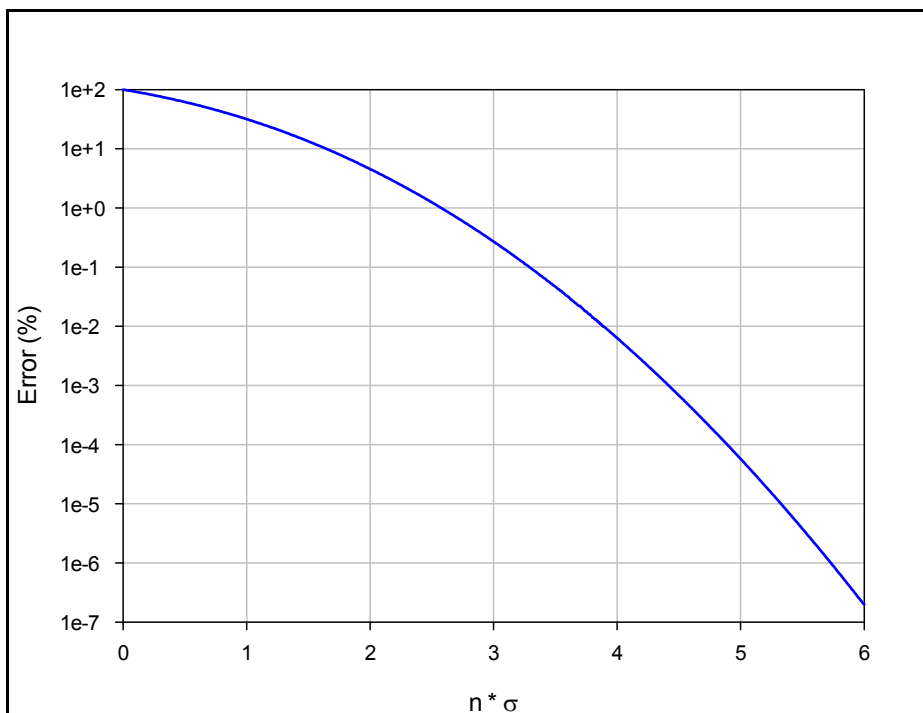
Figure 64: Error Probability as a function of n · σ

We can now define:

- RMS jitter means the jitter value falls within the interval [-σ,σ] which means a probability of about 68%
- Peak-to-Peak jitter means that at an error rate (mostly a bit error rate, BER) of about 10^{-10} which means 99.9999999%, the interval must be about [-6.36σ,6.36σ]. Usually 6σ can be used and this is where "SIX SIGMA" comes from.

If we now define "Period Jitter" as the time difference between a measured cycle period and the set point of the cycle period (ideal value) we can also think of the random variation of the cycle period as a phase noise.

However there is a relationship between Phase Noise and RMS period jitter [14]. Since a square wave has the same phase jitter as its base harmonic. We can then write:

$$f(t) = a\sin[2\pi f_S t + \phi(t)] = a\sin\left[2\pi f_S\left(t + \frac{\phi(t)}{2\pi f_S}\right)\right] \qquad (3.4\text{-}6)$$

The period jitter then equals:

$$jitter_P = \frac{\phi(t)}{2\pi f_S} \qquad (3.4\text{-}7)$$

Since the jitter usually is small compared to the period of the signal and with

$$f(t) = a\sin(2\pi f_S t)\cos(\phi(t)) + a\sin(\phi(t))\cos(2\pi f_S t) \qquad (3.4\text{-}8)$$

$$\sin(\phi(t)) \approx \phi(t) \qquad (3.4\text{-}9)$$

$$\cos(\phi(t)) \approx 1 \qquad (3.4\text{-}10)$$

we can assume f(t):

$$f(t) = a\sin(2\pi f_S t) + a\,\phi(t)\cos(2\pi f_S t) \qquad (3.4\text{-}11)$$

We can calculate the PSD by Fourier transformation with ω=2πf:

$$F(\omega) = aF_1(\omega) + aF_2(\omega) \qquad (3.4\text{-}12)$$

$$F_1(\omega) = i\cdot\pi\cdot[\delta(\omega+\omega_S) - \delta(\omega-\omega_S)] \qquad (3.4\text{-}13)$$

$$F_2(\omega) = \frac{1}{2}\cdot\left[F_\phi(\omega-\omega_S) + F_\phi(\omega+\omega_S)\right] \qquad (3.4\text{-}14)$$

$$S_{xx,i}(\omega) = |aF_i(\omega)|^2, i \in [1,2] \qquad (3.4\text{-}15)$$

$$S_{xx,1}(\omega) = a^2\pi^2[\delta(\omega+\omega_S)^2 - 2\delta(\omega+\omega_S)(\omega-\omega_S) + \delta(\omega-\omega_S)^2] \qquad (3.4\text{-}16)$$

$$S_{xx,1}(\omega) = a^2\pi^2[\delta(\omega+\omega_S) + \delta(\omega-\omega_S)] \qquad (3.4\text{-}17)$$

$$S_{xx,2}(\omega) = \frac{a^2}{4}\left[F_\phi(\omega-\omega_S) + F_\phi(\omega+\omega_S)\right] \qquad (3.4\text{-}18)$$

$$S_{xx,2}(\omega) = \frac{a^2}{4}\left[S_{xx,\phi}(\omega-\omega_S) + S_{xx,\phi}(\omega+\omega_S)\right] \qquad (3.4\text{-}19)$$

$$S_{xx,1}(\omega) \neq 0 \; \forall \; |\omega| = \omega_S \tag{3.4-20}$$

$$S_{xx}(\omega) = S_{xx,1}(\omega) + S_{xx,2}(\omega) \tag{3.4-21}$$

So the PSD of the signal with phase noise is the sum of PSD of the signal and the PSD of the phase noise.

We now define the phase noise spectrum:

$$S_{xx,PN}(\omega) = 10 \log\left[\frac{S_{xx}(\omega + \omega_S)}{S_{xx}(\omega_S)}\right] \tag{3.4-22}$$

The spectral lines are given in dBc. Replacing $S_{xx}(\omega)$ with (3.4-21) shows that:

$$S_{xx,PN}(\omega) = 10 \log\left[S_{xx,\phi}(\omega)\right] \tag{3.4-23}$$

Now at the input of a spectrum analyzer the signal appears as:

$$x(t) = \frac{a}{2}\phi(t) \tag{3.4-24}$$

This can be written as:

$$S_{xx,x}(\omega) = \int_{-\infty}^{\infty} x(t)e^{-i\omega t}dt = \frac{a^2}{4}S_{xx,\phi}(\omega) \tag{3.4-25}$$

$$S_{xx,\phi}(\omega) = \frac{4}{a^2}\int_{-\infty}^{\infty} x(t)e^{-i\omega t}dt = \frac{4}{a^2}S_{xx,x}(\omega) = 10^{\frac{S_{xx,PN}(\omega)}{10}}$$

Since the variance is the integral of the PSD we can write:

$$Var\left(\phi^2(t)\right) = \lim_{N\to\infty}\frac{1}{N}\int_{-\frac{N}{2}}^{\frac{N}{2}}\phi^2(t)dt = 2\int_{0}^{\infty} 10^{\frac{S_{xx,PN}(\omega)}{10}}d\omega \tag{3.4-26}$$

And the relationship between RMS period jitter and phase noise spectrum is:

$$jitter_{P,RMS} = \frac{Var\left(\phi^2(t)\right)}{2\pi\omega_S} = \frac{1}{2\pi\omega_S}\sqrt{2\int_{0}^{\infty} 10^{\frac{S_{xx,PN}(\omega)}{10}}d\omega} \tag{3.4-27}$$

Since the dynamic range of a spectrum analyzer is not high enough to measure $S_{xx,PN}(\omega)$ directly, we must eliminate the spectral energy of the clock frequency ω_S by means of a carrier-suppress demodulator before inputting the signal into the spectrum analyzer.

Do I need all that theory at all? I think yes … it gives an understanding of the problems that arise when you try to measure those quantities. All measuring devices suffer from limited bandwidth, from limited dynamic range and limited signal-to-noise ratio. Also the coupling of the DUT with the measuring device is critical. For jitter measurement you cannot simply attach your scope probe with a 6 inch ground lead to your device under test since the induced noise in the magnetic loop formed by the ground lead may significantly influence your measurement: consider a 10MHz clock with a 1ns rise time and an amplitude of 3.3V. Near to 1.65V (let this be your trigger level) the signal rises with about 2.64V/ns. Consider a 100ps peak-to-peak jitter; this means a ΔV of 0.26V. Any Glitch on the signal around 1.65V with this amplitude can falsely be interpreted as such a jitter due to false triggering. If you use a spectrum

analyzer to measure the phase noise the noise is several decades smaller than the signal as explained earlier. Since jitter measurement means to measure a stochastic variable, at least some understanding of probability theory and stochastic processes: if you want to measure peak-to-peak jitter then 6σ means an error of about 10^{-12}. This means that if you are lucky you will have one event in 10^{12} consecutive trigger events? Deriving peak-to-peak jitter from RMS jitter that has been estimated from a best fit Gaussian distribution to a jitter value histogram is only valid if the sample (the finite measured histogram) represents the underlying stochastic process and this depends on the size of the sample as well. The measured values therefore have to be normal distributed and mean and auto covariance has to be constant and the variance has to be finite (this means steady state or stationarity). Since deterministic jitter is not Gaussian distributed it cannot be characterized by a normal distribution and its moments [15].

If using digital PLLs in a system an understanding how PLLs work and how digital PLLs can introduce phase jitter is beneficial. Since Ethernet PHYs internally use digital PLLs for clock recovery and – for 100Mbit Ethernet - to generate the 125MHz TX clock from 25MHz or 50MHz using a PLL to generate the input clock can lead to funny results!

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