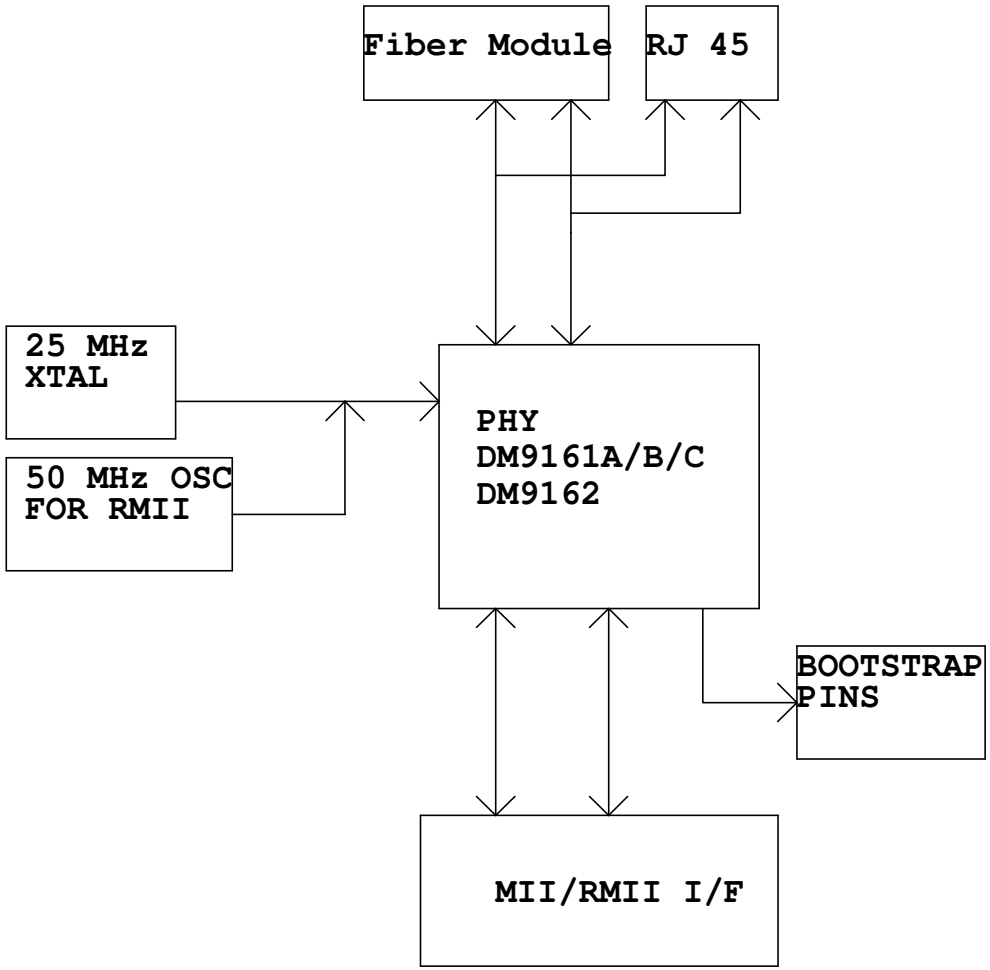
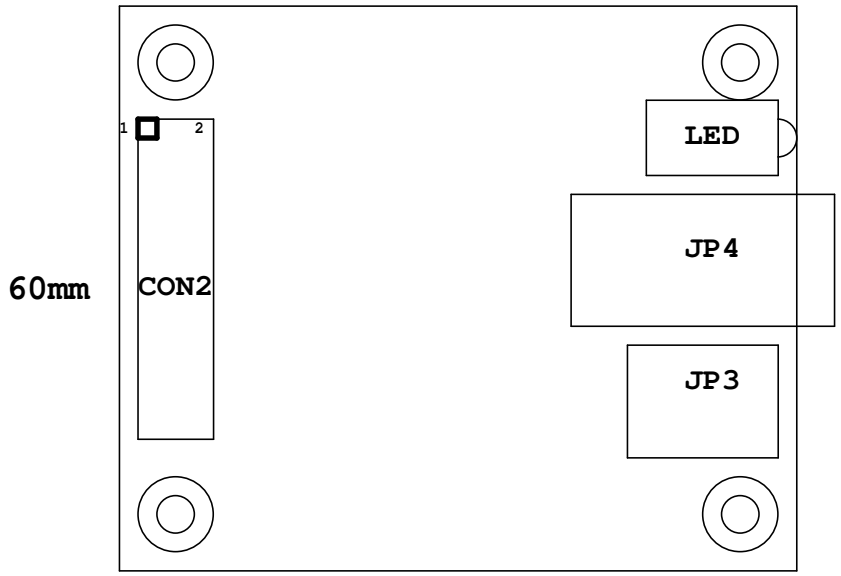
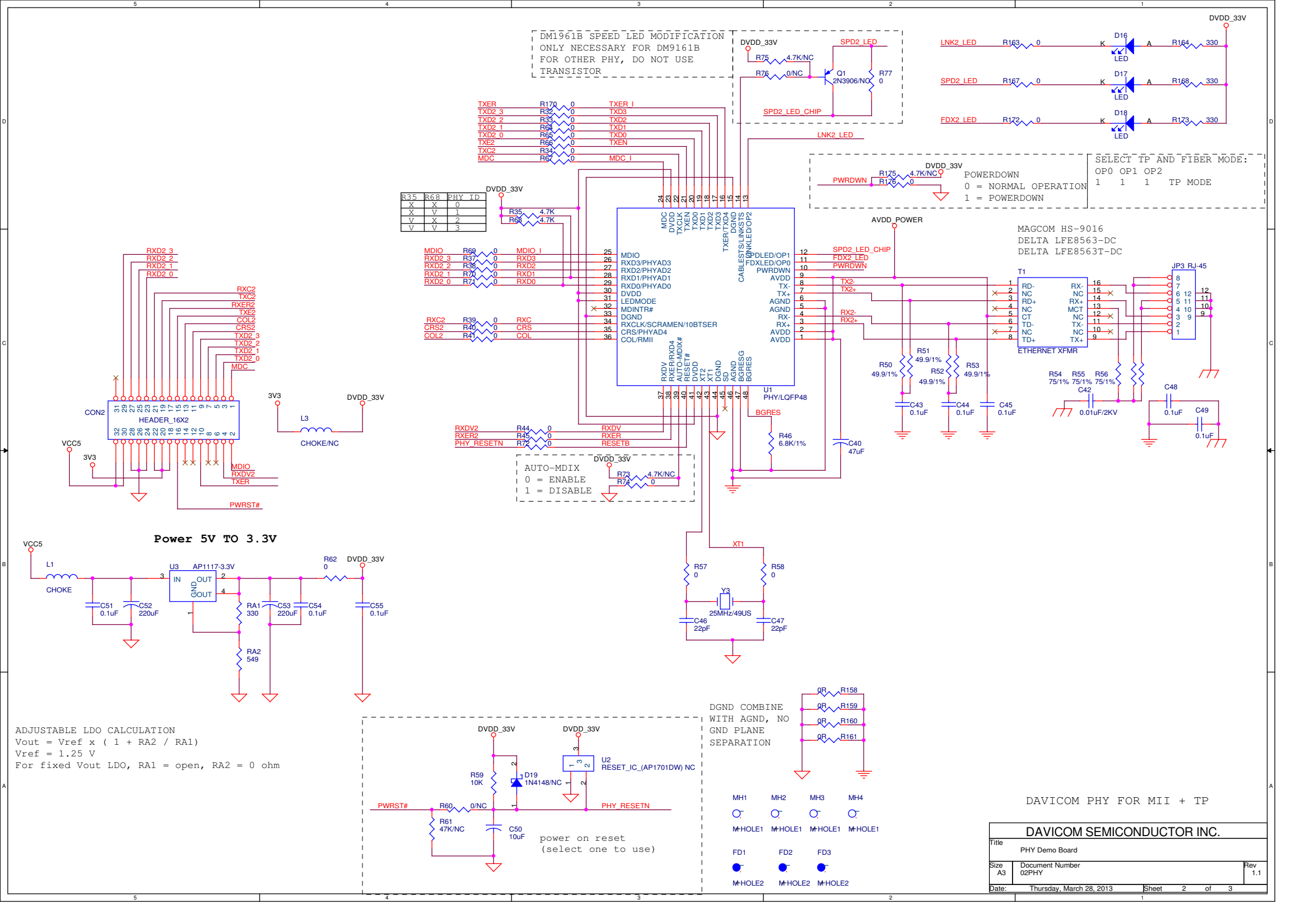
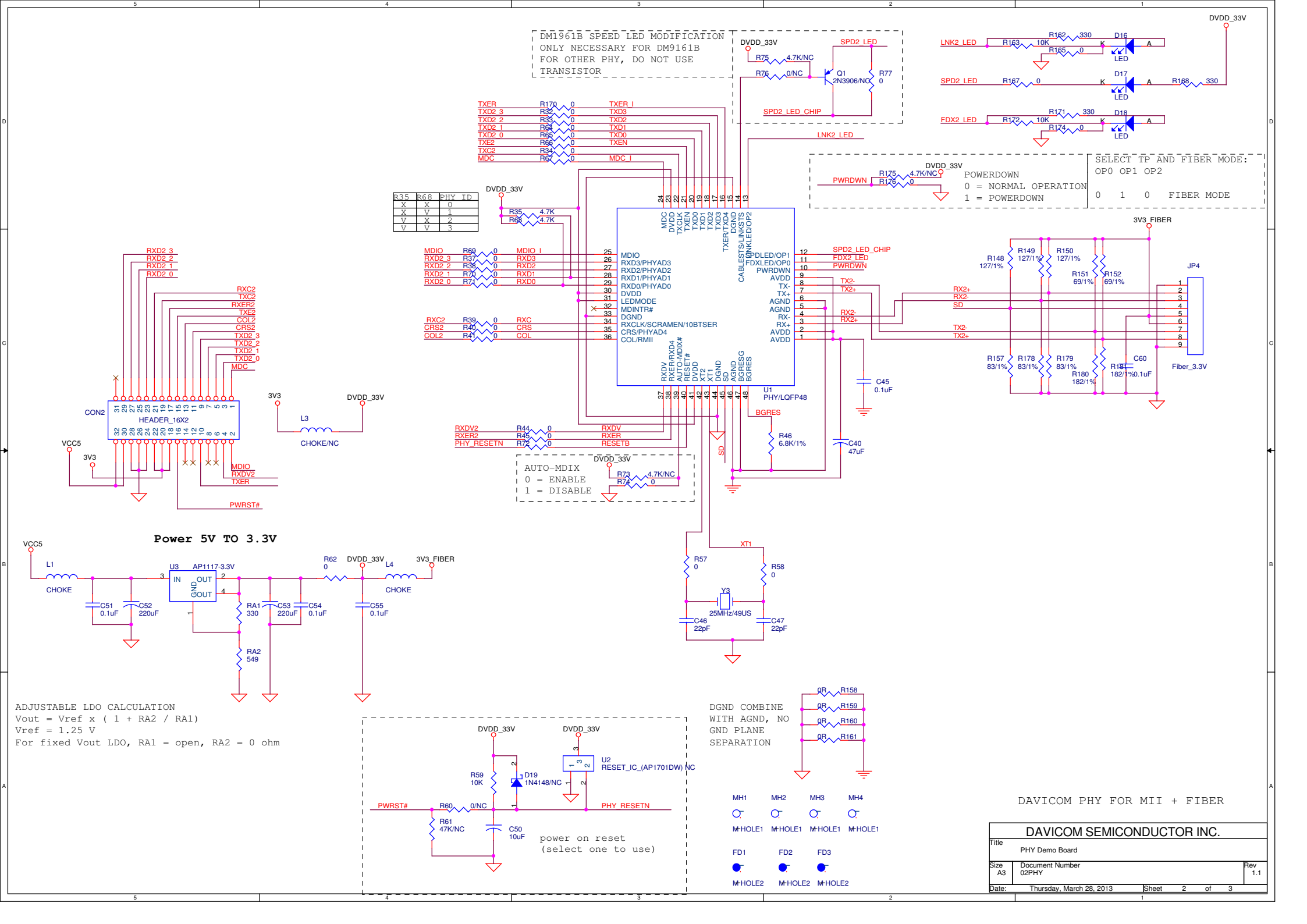


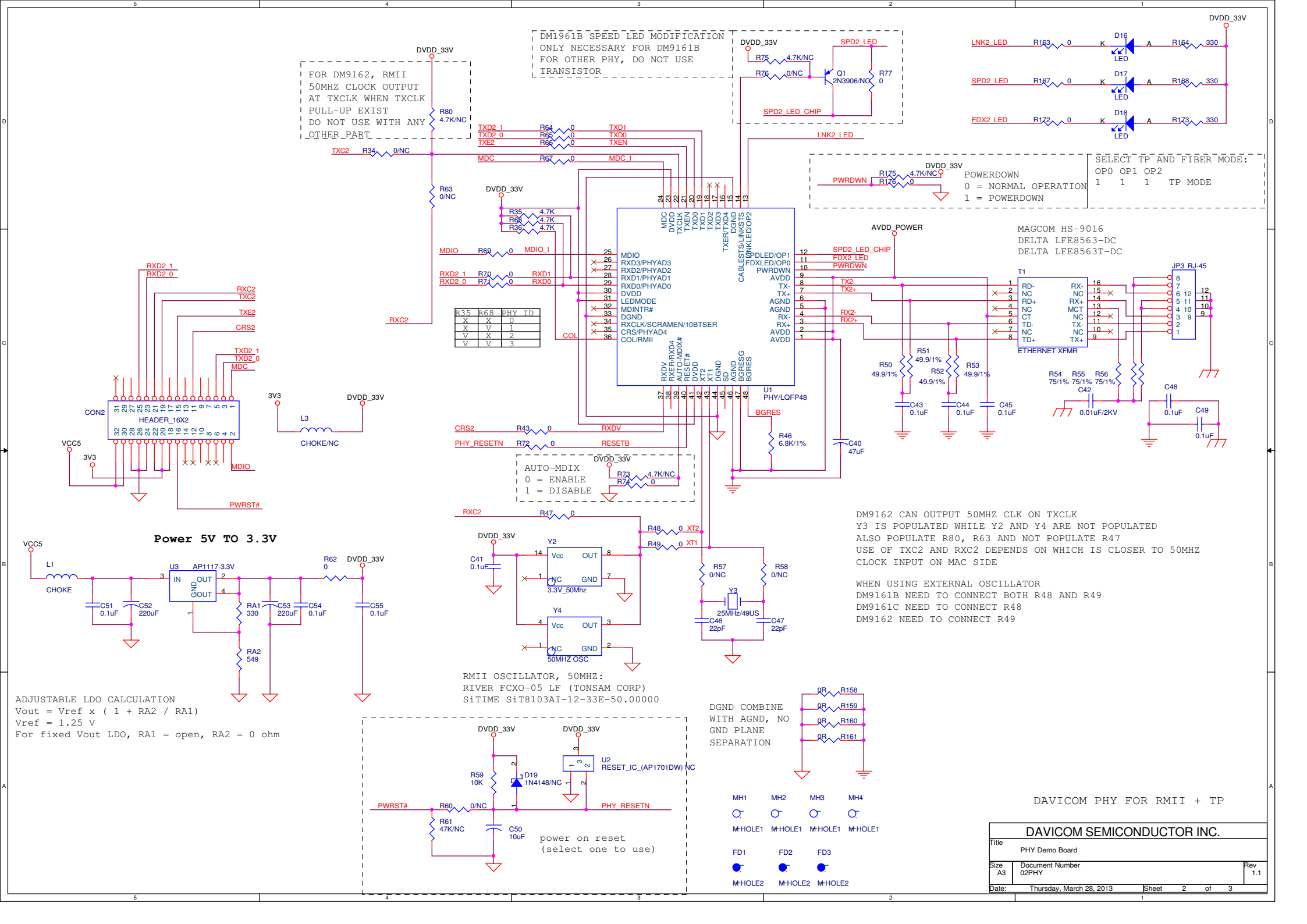


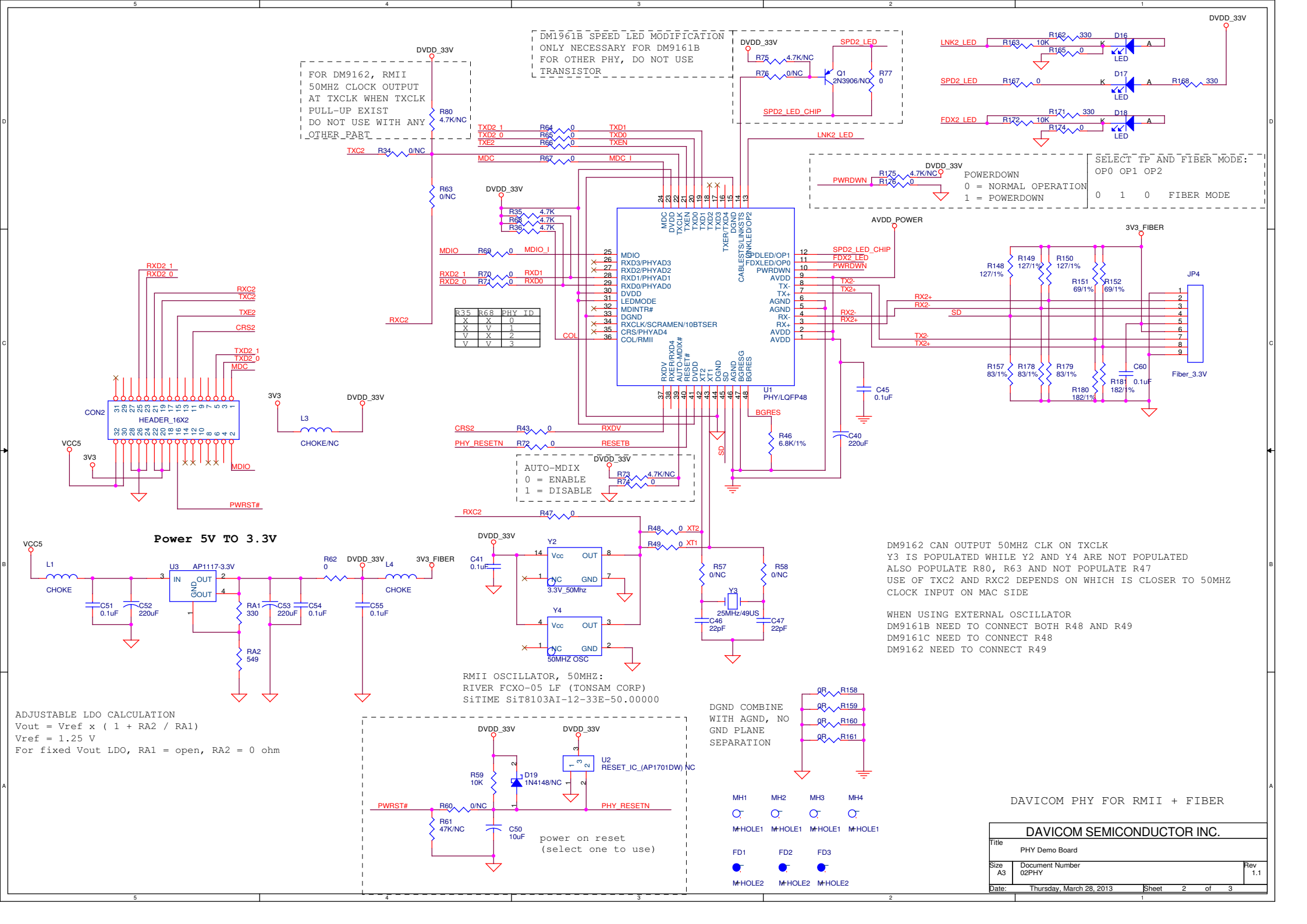
POWER FROM MII
+5V IN
+3.3V OUT
POWER
+3.3V IN
+1.8V OUT

Davicom Semiconductor Inc.		
Title: PHY Demo Board (PCB_Overview)		
Size: A4	Document Number: 01TOP	Rev: 1.1
Date: Thursday, March 28, 2013	Sheet 1 of 3	


DM1961B SPEED LED MODIFICATION
ONLY NECESSARY FOR DM9161B
FOR OTHER PHY, DO NOT USE
TRANSISTOR
DVDD_33V
SPD2_LED
R75 4.7K/NC
R76 0/NC
Q1 2N3906/NC
R77 0
SPD2_LED_CHIP
LNK2_LED
SPD2_LED
FDX2_LED
D16 LED
D17 LED
D18 LED
R163 0
R164 330
R167 0
R168 330
R172 0
R173 330
TXER R170 0 TXER_I
TXD2_3 R32 0 TXD3
TXD2_2 R33 0 TXD2
TXD2_1 R64 0 TXD1
TXD2_0 R65 0 TXD0
TXE2 R66 0 TXEN
TXC2 R34 0
MDC R67 0 MDC_I
R35 R68 PHY_ID
X X 0
X V 1
V X 2
V V 3
R35 4.7K
R68 4.7K
PWRDWN
R175 4.7K/NC
R176 0
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
1 1 1 TP MODE
MDIO R69 0 MDIO_I
RXD2_3 R37 0 RXD3
RXD2_2 R38 0 RXD2
RXD2_1 R70 0 RXD1
RXD2_0 R71 0 RXD0
RXC2 R39 0 RXC
CRS2 R40 0 CRS
COL2 R41 0 COL
MDIO
RXD3/PHYAD3
RXD2/PHYAD2
RXD1/PHYAD1
RXD0/PHYAD0
DVDD
LEDMODE
MDINTR#
DGND
RXCLK/SCRAMEN/10BTSER
CRS/PHYAD4
COL/RMII
RXDV
RXER/RXD4
AUTO-MDIX#
RESET#
DVDD
XT2
XT1
DGND
SD
AGND
BGRESG
BGRES
MDC
DVDD
TXCLK
TXEN
TXD0
TXD1
TXD2
TXD3
TXER/TXD4
DGND
LINKSTS
LNKLEDOP2
CABLESTS/LINKSTS
SPDLED/OP1
FDXLED/OP0
PWRDWN
AVDD
TX-
TX+
AGND
AGND
RX-
RX+
AVDD
AVDD
U1 PHY/LQFP48
BGRES
R46 6.8K/1%
C40 47uF
RXDV2 R44 0 RXDV
RXER2 R45 0 RXER
PHY_RESETN R72 0 RESETB
AUTO-MDIX
0 = ENABLE
1 = DISABLE
R73 4.7K/NC
R74 0
AVDD_POWER
SPD2_LED_CHIP
FDX2_LED
PWRDWN
TX2-
TX2+
RX2-
RX2+
MAGCOM HS-9016
DELTA LFE8563-DC
DELTA LFE8563T-DC
T1
RD-
NC
RD+
NC
CT
TD-
NC
TD+
RX-
NC
RX+
MCT
TX-
NC
TX+
ETHERNET XFMR
JP3 RJ-45
R50 49.9/1%
R51 49.9/1%
R52 49.9/1%
R53 49.9/1%
R54 75/1%
R55 75/1%
R56 75/1%
C42 0.01uF/2KV
C43 0.1uF
C44 0.1uF
C45 0.1uF
C48 0.1uF
C49 0.1uF
RXD2_3
RXD2_2
RXD2_1
RXD2_0
RXC2
TXC2
RXER2
TXE2
COL2
CRS2
TXD2_3
TXD2_2
TXD2_1
TXD2_0
MDC
CON2
HEADER_16X2
VCC5
3V3
MDIO
RXDV2
TXER
PWRST#
3V3
L3
CHOKE/NC
DVDD_33V
Power 5V TO 3.3V
VCC5
L1
CHOKE
U3 AP1117-3.3V
IN
OUT
GND
GOUT
C51 0.1uF
C52 220uF
RA1 330
RA2 549
C53 220uF
C54 0.1uF
R62 0
C55 0.1uF
DVDD_33V
XT1
R57 0
R58 0
Y3
25MHz/49US
C46 22pF
C47 22pF
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open, RA2 = 0 ohm
DVDD_33V
DVDD_33V
R59 10K
D19 1N4148/NC
U2 RESET_IC_(AP1701DW) NC
PWRST#
R60 0/NC
PHY_RESETN
R61 47K/NC
C50 10uF
power on reset
(select one to use)
DGND COMBINE
WITH AGND, NO
GND PLANE
SEPARATION
0R R158
0R R159
0R R160
0R R161
MH1
MH2
MH3
MH4
M-HOLE1
FD1
FD2
FD3
M-HOLE2
DAVICOM PHY FOR MII + TP
DAVICOM SEMICONDUCTOR INC.
Title
PHY Demo Board
Size A3
Document Number 02PHY
Rev 1.1
Date: Thursday, March 28, 2013
Sheet 2 of 3


DM1961B SPEED LED MODIFICATION
ONLY NECESSARY FOR DM9161B
FOR OTHER PHY, DO NOT USE
TRANSISTOR
DVDD_33V
R75 4.7K/NC
R76 0/NC
Q1 2N3906/NC
R77 0
SPD2_LED
SPD2_LED_CHIP
LNK2_LED
FDX2_LED
R162 330
R163 10K
R165 0
R167 0
R168 330
R171 330
R172 10K
R174 0
D16
D17
D18
LED
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
0 1 0 FIBER MODE
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
PWRDWN
R175 4.7K/NC
R176 0
R35 4.7K
R68 4.7K
R35 R68 PHY_ID
X X 0
X V 1
V X 2
V V 3
U1
PHY/LQFP48
MDC
MDIO
RXD3/PHYAD3
RXD2/PHYAD2
RXD1/PHYAD1
RXD0/PHYAD0
DVDD
LEDMODE
MDINTR#
DGND
RXCLK/SCRAMEN/10BTSER
CRS/PHYAD4
COL/RMII
RXDV
RXER/RXD4
AUTO-MDIX#
RESET#
XT2
XT1
AGND
BGRES
TXER
TXD3
TXD2
TXD1
TXD0
TXEN
MDC_I
TXER_I
RXD3
RXD2
RXD1
RXD0
RXC
CRS
COL
RXDV
RXER
RESETB
BGRES
R46 6.8K/1%
C45 0.1uF
C40 47uF
AUTO-MDIX
0 = ENABLE
1 = DISABLE
R73 4.7K/NC
R74 0
3V3_FIBER
JP4
Fiber_3.3V
R148 127/1%
R149 127/1%
R150 127/1%
R151 69/1%
R152 69/1%
R157 83/1%
R178 83/1%
R179 83/1%
R180 182/1%
R181 182/1%
C60 0.1uF
CON2
HEADER_16X2
VCC5
3V3
L3
CHOKE/NC
PWRST#
Power 5V TO 3.3V
U3 AP1117-3.3V
L1 CHOKE
L4 CHOKE
R62 0
C51 0.1uF
C52 220uF
C53 220uF
C54 0.1uF
C55 0.1uF
RA1 330
RA2 549
XT1
Y3 25MHz/49US
R57 0
R58 0
C46 22pF
C47 22pF
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open, RA2 = 0 ohm
U2
RESET_IC_(AP1701DW) NC
D19 1N4148/NC
R59 10K
R60 0/NC
R61 47K/NC
C50 10uF
power on reset
(select one to use)
DGND COMBINE
WITH AGND, NO
GND PLANE
SEPARATION
R158 0R
R159 0R
R160 0R
R161 0R
MH1 MH2 MH3 MH4
M-HOLE1
FD1 FD2 FD3
M-HOLE2
DAVICOM PHY FOR MII + FIBER
DAVICOM SEMICONDUCTOR INC.
Title PHY Demo Board
Size A3
Document Number 02PHY
Rev 1.1
Date: Thursday, March 28, 2013
Sheet 2 of 3


DM1961B SPEED LED MODIFICATION
ONLY NECESSARY FOR DM9161B
FOR OTHER PHY, DO NOT USE
TRANSISTOR
FOR DM9162, RMII
50MHZ CLOCK OUTPUT
AT TXCLK WHEN TXCLK
PULL-UP EXIST
DO NOT USE WITH ANY
OTHER PART
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
1 1 1 TP MODE
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
MAGCOM HS-9016
DELTA LFE8563-DC
DELTA LFE8563T-DC
AUTO-MDIX
0 = ENABLE
1 = DISABLE
Power 5V TO 3.3V
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open, RA2 = 0 ohm
RMII OSCILLATOR, 50MHZ:
RIVER FCXO-05 LF (TONSAM CORP)
SiTIME SiT8103AI-12-33E-50.00000
DM9162 CAN OUTPUT 50MHZ CLK ON TXCLK
Y3 IS POPULATED WHILE Y2 AND Y4 ARE NOT POPULATED
ALSO POPULATE R80, R63 AND NOT POPULATE R47
USE OF TXC2 AND RXC2 DEPENDS ON WHICH IS CLOSER TO 50MHZ
CLOCK INPUT ON MAC SIDE
WHEN USING EXTERNAL OSCILLATOR
DM9161B NEED TO CONNECT BOTH R48 AND R49
DM9161C NEED TO CONNECT R48
DM9162 NEED TO CONNECT R49
DGND COMBINE
WITH AGND, NO
GND PLANE
SEPARATION
power on reset
(select one to use)
DAVICOM PHY FOR RMII + TP
DAVICOM SEMICONDUCTOR INC.
Title PHY Demo Board
Size A3
Document Number 02PHY
Rev 1.1
Date: Thursday, March 28, 2013
Sheet 2 of 3


DM1961B SPEED LED MODIFICATION
ONLY NECESSARY FOR DM9161B
FOR OTHER PHY, DO NOT USE
TRANSISTOR
FOR DM9162, RMII
50MHZ CLOCK OUTPUT
AT TXCLK WHEN TXCLK
PULL-UP EXIST
DO NOT USE WITH ANY
OTHER PART
SELECT TP AND FIBER MODE:
OP0 OP1 OP2
0 1 0 FIBER MODE
POWERDOWN
0 = NORMAL OPERATION
1 = POWERDOWN
AUTO-MDIX
0 = ENABLE
1 = DISABLE
Power 5V TO 3.3V
ADJUSTABLE LDO CALCULATION
Vout = Vref x (1 + RA2 / RA1)
Vref = 1.25 V
For fixed Vout LDO, RA1 = open, RA2 = 0 ohm
RMII OSCILLATOR, 50MHZ:
RIVER FCXO-05 LF (TONSAM CORP)
SiTIME SiT8103AI-12-33E-50.00000
power on reset
(select one to use)
DGND COMBINE
WITH AGND, NO
GND PLANE
SEPARATION
DM9162 CAN OUTPUT 50MHZ CLK ON TXCLK
Y3 IS POPULATED WHILE Y2 AND Y4 ARE NOT POPULATED
ALSO POPULATE R80, R63 AND NOT POPULATE R47
USE OF TXC2 AND RXC2 DEPENDS ON WHICH IS CLOSER TO 50MHZ
CLOCK INPUT ON MAC SIDE
WHEN USING EXTERNAL OSCILLATOR
DM9161B NEED TO CONNECT BOTH R48 AND R49
DM9161C NEED TO CONNECT R48
DM9162 NEED TO CONNECT R49
DAVICOM PHY FOR RMII + FIBER
DAVICOM SEMICONDUCTOR INC.
Title
PHY Demo Board
Size A3
Document Number 02PHY
Rev 1.1
Date: Thursday, March 28, 2013
Sheet 2 of 3

VER	DATE	ENGINEER	NOTE
1.0	12/12/2007	WILLIE NIOU	INITAL CIRCUIT CREATION
1.1	4/12/2010	WILLIE NIOU	BUG FIX AND ENHANCEMENTS: 1. CON2 GND CONNECT TO BOARD GND 2. LED LAYOUT LIBRARY NOT SAME AS ACUTAL COMPONENT USED. NEED TO CHANGE DIRECTION 180 DEGREES 3. C42 NEED TO CONNECT PIN 2 AND 3 TOGETHER 4. AGND AND DGND CONNECTED 5. ADD SPEED LED CONTROL CIRCUIT, DUE TO DM9161B DESIGN 6. ADD EXTERNAL 1.8V LDO FOR INPUT TO CENTER TAP OF TRANSFORMER TO REDUCE HEAT DISSIPATION BY CHIP
	2011/7/5	ALLIANG	1: ADD Fiber Module and termination circuit 2: CN2 MII Connector change to 16*2 Pinch 2.54mm 3: Change LED Anode & Cathode 4: Add R63,R80 For TXCLK and RXCLK wire link

Davicom Semiconductor Inc.

Title: PHY Demo Board (History)		
Size: A4	Document Number: HISTORY	Rev: 1.1
Date: Thursday, March 28, 2013	Sheet 3 of 3	