DM9161B

Layout Guide

Version: 1.1

Technical Reference Manual
Davicom Semiconductor, Inc
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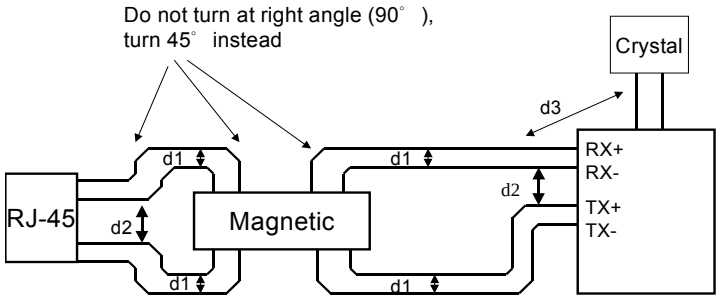
1. Placement, Signal and Trace Routing

- Place the Ethernet transformer as close as possible to the DM9161B (no more than 20mm) and to the RJ-45 connector.
- Place the termination resistors, 50Ω, as close as possible to the DM9161B RX± pins and TX± pins. The 50 Ω resistors and grounding capacitors of TX± and RX± should be placed near DM9161 with no more than 10mm separation.
- The 25MHz crystal should not be placed near important signal traces, such as RX± receive pair and TX± transmit pair, band gap resistor, magnetic and board edge.
- Traces routed from the DM9161B RX± pair to the Ethernet transformer and the RJ45 connector should run symmetrically, closely (no more than 2mm gap between the two lines) and shortest distance. The same rule is applicable to traces routed from the DM9161B TX± pair.

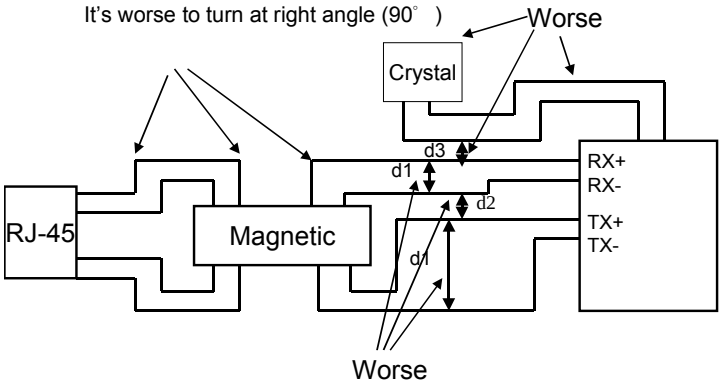


better

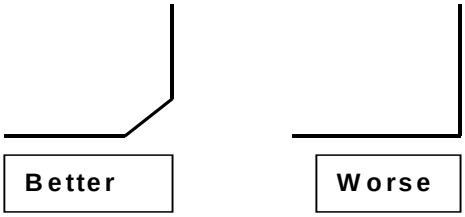
d1 < 2mm

d2 > 3mm; having AGND as a shield is better

d3 > 5mm; having AGND as a shield is better



- It is recommended that RX± receive and TX± transmit traces turn at 45° angle. Do not turn at right angle.



- Avoid using vias in routing the traces of RX± pair and TX± pair.
- The RX± pair and TX± pair traces should be routed with differential impedance of 100 Ohm. The clock trace should be routed with impedance of 50 Ohm.
- Do not cross the DM9161B RX± traces and the TX± traces. Keep the receive pair, RX±, away from the transmit pair, TX±, with more than 3mm between them. It's better to place ground plane between these two pairs of traces.
- Do not route any digital signal in the area between the DM9161B RX± and TX± pairs to the RJ-45. Keep the two pairs away from all the other active signals and the chassis ground.
- No power and ground planes in the area between the Ethernet transformer and the RJ-45 connector.
- Any terminated pins of the RJ-45 connector (pins 4,5,7 and 8) and the Ethernet transformer should be tied to the chassis ground through a resistor network of 75Ω resistors and a 0.01μF/2KV bypass capacitor within 2mm of the Ethernet transformer.
- The Band Gap resistor should be placed as close as possible to pins 47 and 48 (BGRES, BGRESG) with less than 3mm distance from pin. Avoid running any high-speed signal near the Band Gap resistor placement.

10Base-T/100Base-TX Application

Figure 1-1 and 1-2 illustrate the two types of the specific magnetic interconnect and how to connect with Davicom DM9161B. These magnetic are not pin-to-pin compatible.

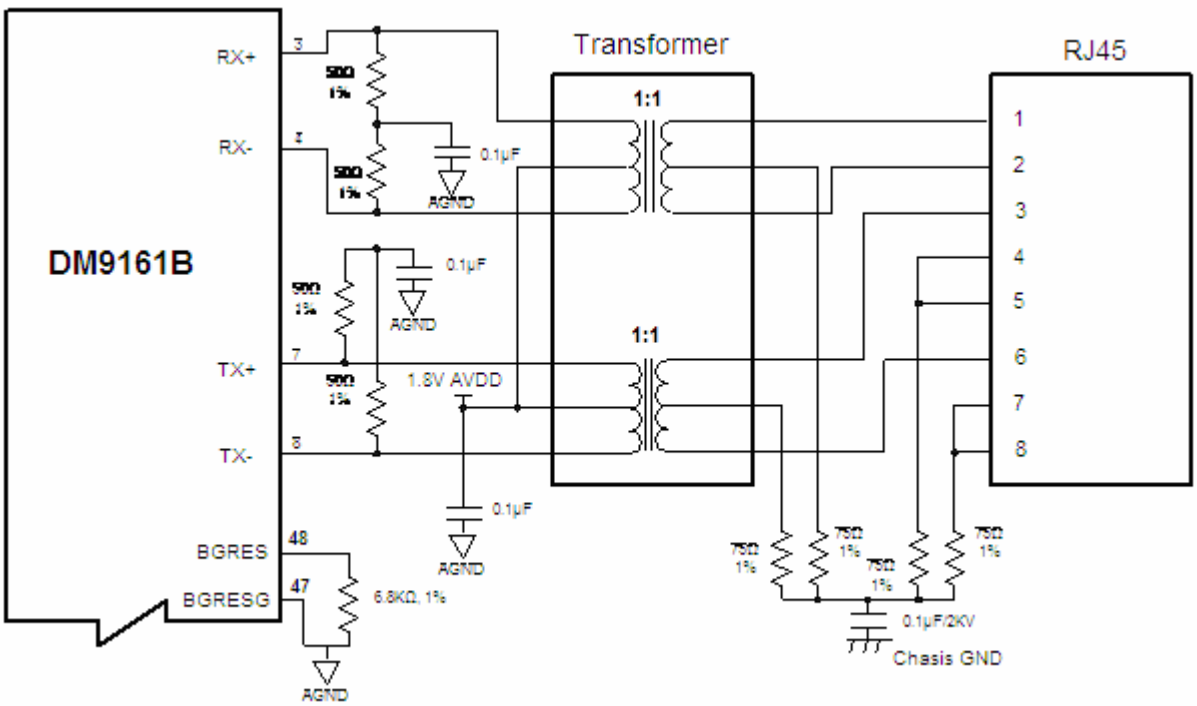


Figure 1-1

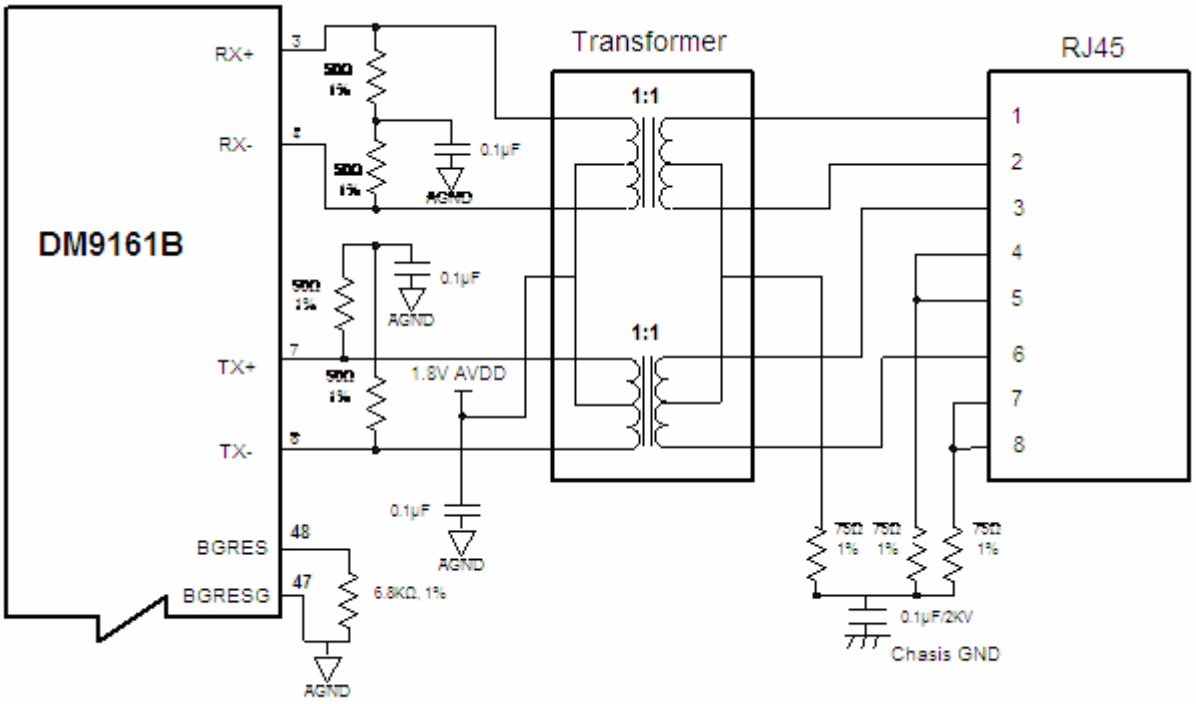


Figure 1-2

2. Power Supply Decoupling Capacitors

- Place all of the decoupling capacitors for all power supply pins as close as possible to the power pins of the DM9161B with no more than 2.5mm from the above power pins. The recommended decoupling capacitor is either 0.1µF or 0.01µF.
- The PCB layout and power supply decoupling should provide sufficient decoupling to achieve the following when measured at the device:
  (1) All DVDDs and AVDDs should be within 50mVpp of each other,
  (2) All DGNDs and AGNDs should be within 50mVpp of each other.
  (3) The resultant ripple noise voltage measured across each DVDD/DGND set and AVDD/AGND set should be less than 100m Vpp.
- The 0.1-0.01µF decoupling capacitor should be connected between each DVDD/DGND set and AVDD/AGND set and be placed as close as possible to the pins of DM9161B. The conservative approach is to use two decoupling capacitors on each DVDD/DGND set and AVDD/AGND set. One 0.1µF is for low frequency noise, and the other 0.01µF is for high frequency noise on the power supply.
- The AVDD connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01µF decoupling capacitor should be placed between the center tap AVDD to AGND ground plane. This decoupling capacitor should be placed as close as possible to the center tap of the magnetic.10 uF or 47 uF Capacitor should be connected between each AVDD and AGND.

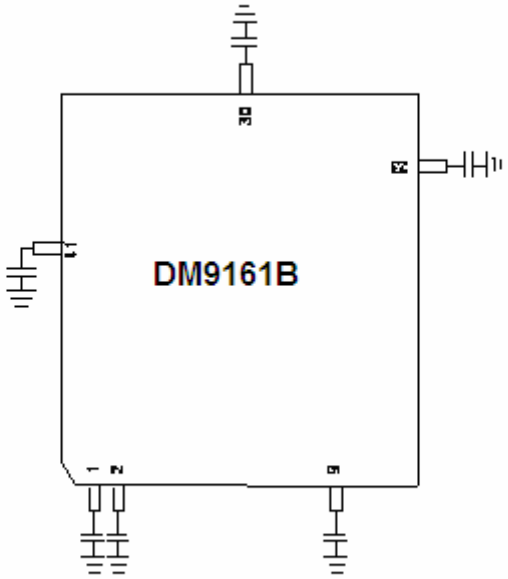


Figure 2

3. Ground Plane Layout

- The combination of AGND and DGND means that there is only ONE ground plane.
- The use of a single ground plane helps to minimize EMI. Ground plane partitioning can cause increased EMI emissions that could make the network interface card (NIC) not comply with specific FCC part 15 and CE regulations.

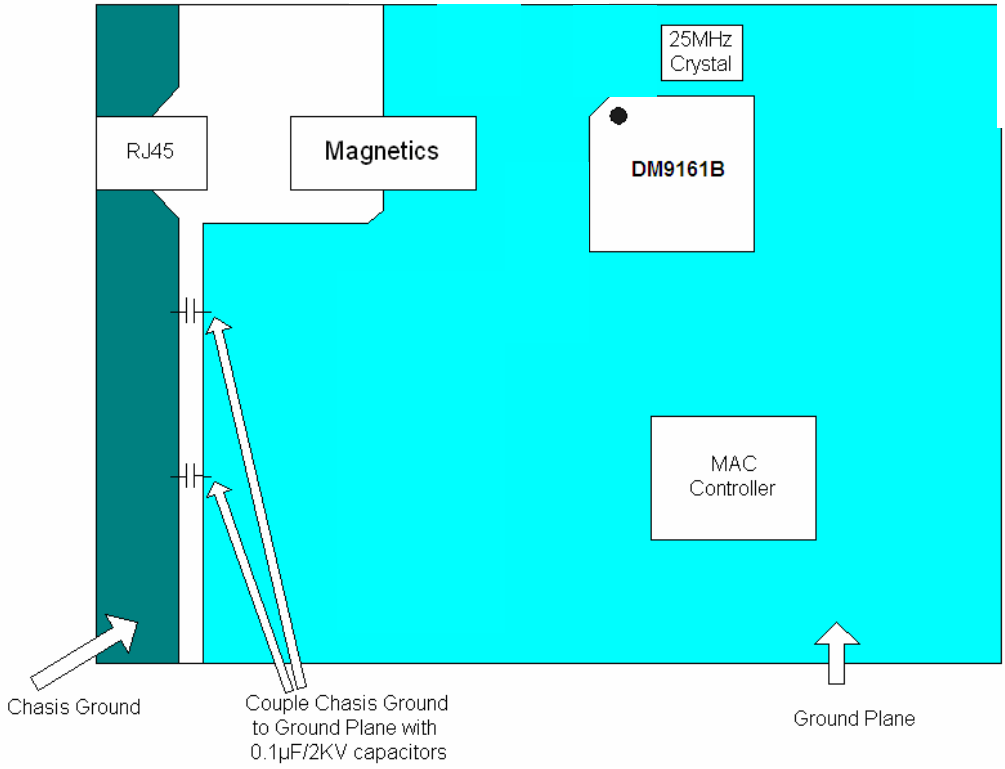


Figure 3-1

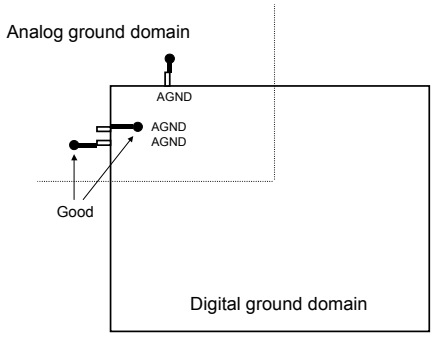


Figure 3-2

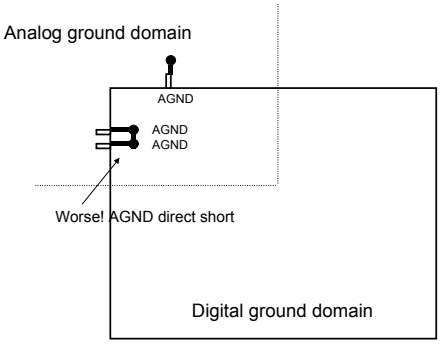


Figure 3-3

4. Power Plane Partitioning

- The power planes should be approximately illustrated in Figure 4. The ferrite bead used should have an impedance 100Ω at 100MHz and at least 200mA. A suitable bead is the Panasonic surface mound bead, part number EXCCL4532U. A 10μF, 0.1μF and 0.01μF bypass capacitors should be connected between VDD and GND at the device side of each of the ferrite bead.
- Separate analog power planes from noisy digital power planes.

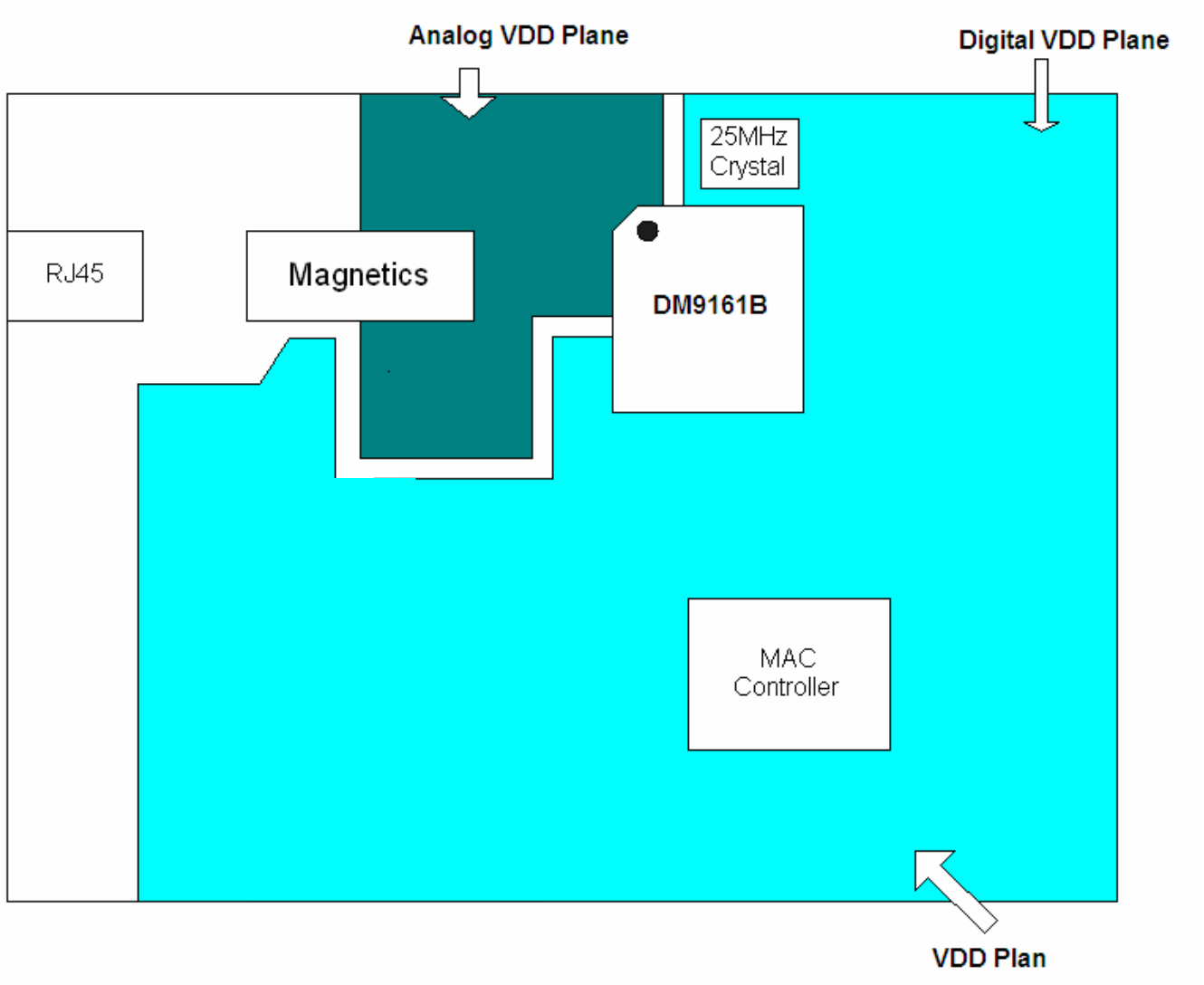


Figure 4

5. Magnetics Selection Guide

- Refer to the following tables 5-1 and 5-2 for Ethernet transformer sources and specification requirements. The magnetics which meet these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetics listed in the following table are electrical equivalents, but may not be pin-to-pin equivalents.

Manufacturer	Part Number
MAGCOM`	HS9016, HS9024
Delta	LFE8563-DC, LFE8563T-DC
Pulse Engineering	PE-68515, H1102
YCL	PH163112, PH163539
Halo	TG110-S050N2, TG110-LC50N2
Bel Fuse	S558-5999-W2
GTS	FC-618SM

Table 5-1: Ethernet transformers Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	μH (Min)	-
Insertion loss	1.1	dB (Max)	1 – 100 MHz
Return loss	-18	dB (Min)	1 –30 MHz
	-14	dB (Min)	30 – 60 MHz
	-12	dB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	dB (Min)	1 – 60 MHz
	-30	dB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

Table 5-2: Magnetic Specification Requirements

6. Crystal Selection Guide

- A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, series-resonant, connect to XT1 and XT2, and shunt each crystal lead to ground with a 22pF capacitor as shown in Figure 6.

PARAMETER	SPEC
Type	Fundamental, series-resonant
Frequency	25 MHz +/- 0.01%
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.

Table 6-1: Crystal Specifications

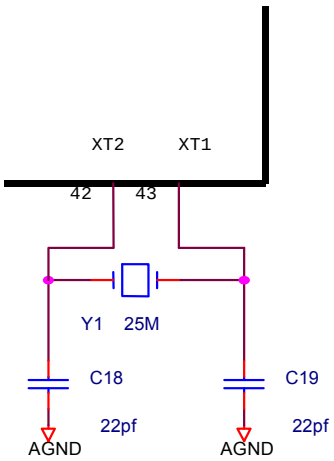


Figure 6
Crystal Circuit Diagram

7. MII Signals to Mac Controller

- The length of the trace routing for the Media Independent Interface (MII) signals should be as short and direct as possible between the DM9161B and MAC controller with no more than 20cm apart. These MII signals are as follows,

  CRS, COL, TXD3, TXD2, TXD1, TXD0, TXEN, TXCLK, TXER
  RXER, RXCLK, RXDV, RXD0, RXD1, RXD2, RXD3, MDC, MDIO

- TXD [0-3] and TXCLK length mismatch does not exceed 2cm.
- RXD [0-3] and RXCLK length mismatch does not exceed 2cm.
- All signal trace should be considered to have characteristic impedance of 50 Ohm.