DM9162

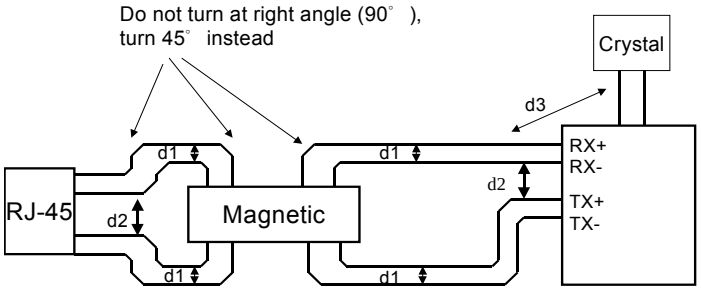
Layout Guide

Version: 1.0

Technical Reference Manual
Davicom Semiconductor, Inc
January 3, 2012

1. Placement, Signal and Trace Routing

- Place the 10/100M magnetic as close as possible to the DM9162 (no more than 20mm) and to the RJ-45 connector.
- Place the termination resistors 50Ω as close as possible to the 10/100M magnetic and the DM9162 RX± pins and TX± pins. The 50Ω resistors and grounding capacitors of TX± and RX± should be placed near DM9161 (no more than 10mm).
- The 25MHz crystal should not be placed near important signal traces, such as RX± receive pair and TX± transmit pair, band gap resistor, magnetic and board edge.
- Traces routed from the DM9162 RX± pair to the 10/100M magnetic and the RJ45 connector should run symmetrically, directly, identically, and closely (no more than 2mm). The same rule is applied to traces routed from the DM9162 TX± pair.

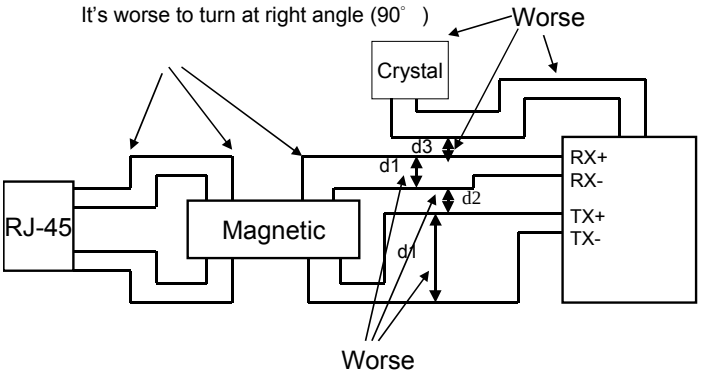


better

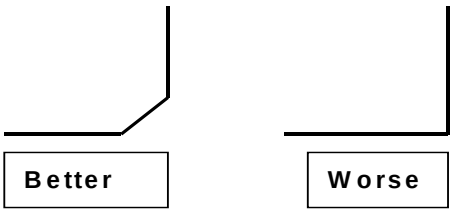
d1 < 2mm

d2 > 3mm; having AGND as a shield is better

d3 > 5mm; having AGND as a shield is better



- It is recommended that RX± receive and TX± transmit traces turn at 45° angle. Do not turn at right angle.



- Avoid using vias in routing the traces of RX± pair and TX± pair.
- The RX± pair, TX± pair, clock, should be routed to have characteristic impedance of 50 Ohm.
- Do not place the DM9162 RX± receive pair across the TX± transmit pair. Keep the receive pair away from the transmit pair (no less than 3mm). It's better to place ground plane between these two pairs of traces.
- The network interface (see Figure 3-1 and Figure 4) does not route any digital signal between the DM9162 RX± and TX± pairs to the RJ-45. Keep the two pairs away from all the other active signals and the chassis ground.
- It should be no power or ground plane in the area under the network side of the 10/100M magnetic and the area under the RJ-45 connector.
- Any terminated pins of the RJ-45 connector (pins 4,5,7 and 8, see Figure 1) and the magnetic (see Figure 1) should be tied as closely as possible to the chassis ground through a resistor divider network 75Ω resistors (no more than 2mm to the magnetic) and a 0.01μF/2KV bypass capacitor.
- The Band Gap resistor should be placed as close as possible to pins 47 and 48 (BGRES, BGRESG) (no more than 3mm). Avoid running any high-speed signal near the Band Gap resistor placement (no less than 3mm from 25MHz XT1 and XT2).

10Base-T/100Base-TX Application

Figure 1-1 and 1-2 illustrate the two types of the specific transformer interconnects and how to connect with Davicom DM9162. These two transformers are not pin-to-pin compatible and must be considered when using the DM9162 in auto-MDIX mode.

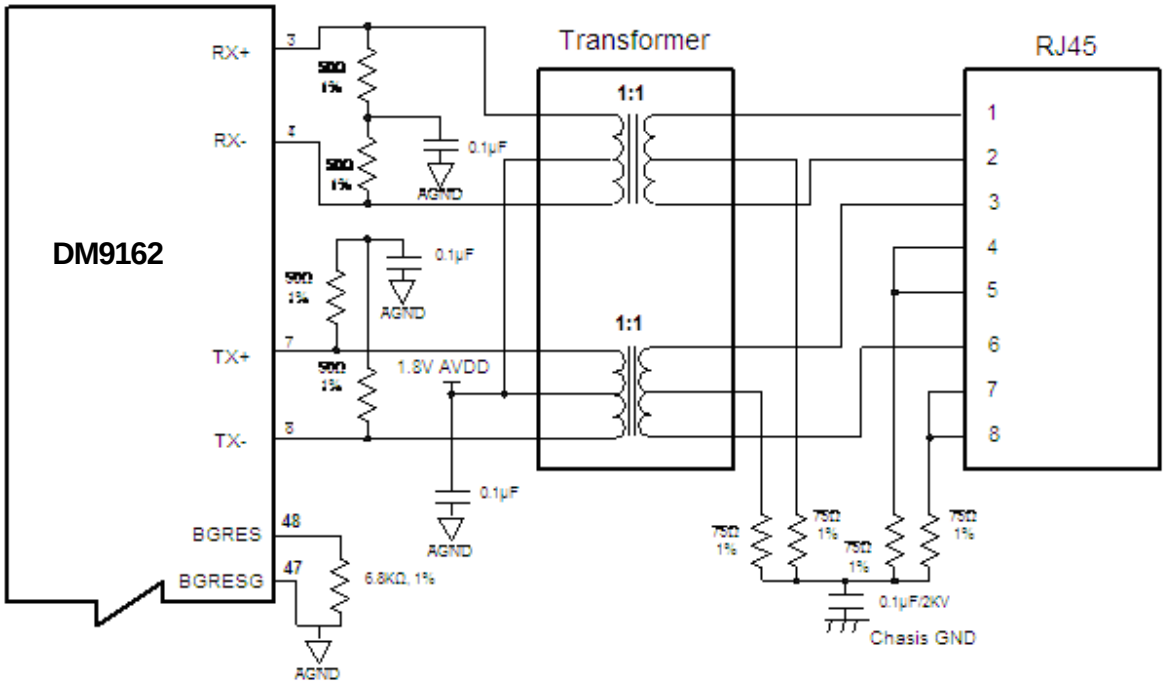


Figure 1-1

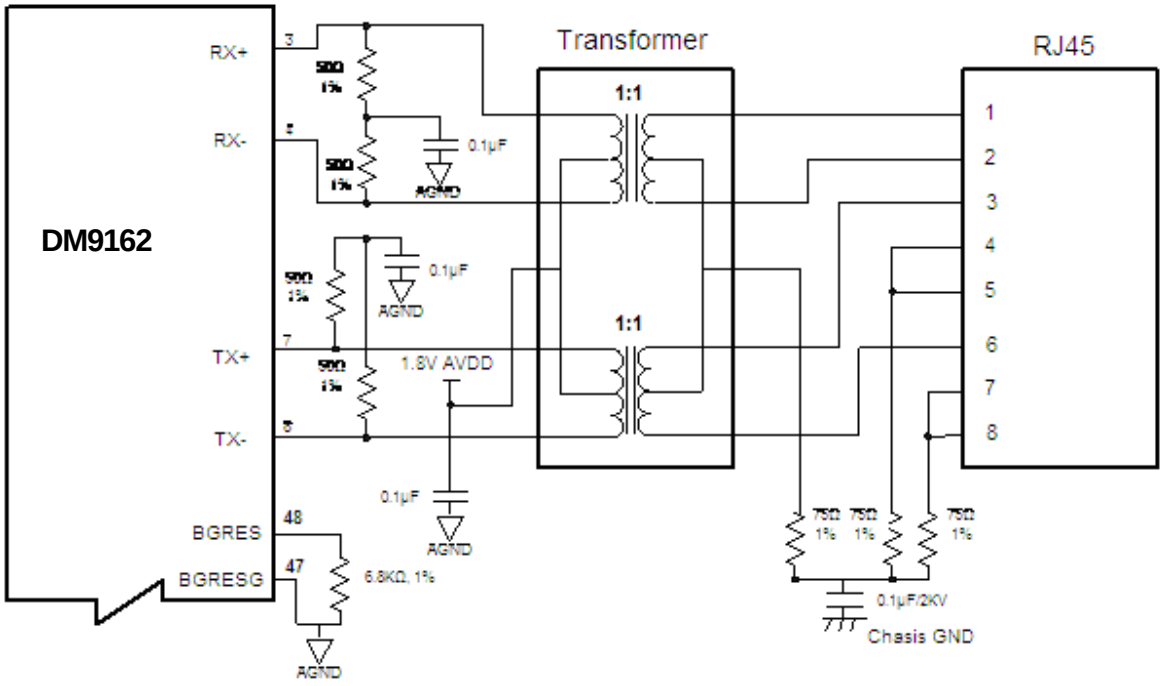


Figure 1-2

2. Power Supply Decoupling Capacitors

- Place all the decoupling capacitors for all power supply pins as close as possible to the power pads of the DM9162 (no more than 2.5mm from the above mentioned pins). The recommended decoupling capacitor is 0.1μF or 0.01μF.
- The PCB layout and power supply decoupling should provide sufficient decoupling to achieve the following when measured at the device:
  (1) All DVDDs and AVDDs should be within 50mV peak to peak of each other,
  (2) All DGNDs and AGNDs should be within 50mV peak to peak of each other.
  (3) The resultant AC noise voltage measured across each DVDD/DGND set and AVDD/AGND set should be less than 100mV peak to peak.
- The 0.1-0.01μF decoupling capacitor should be connected between each DVDD/DGND set and AVDD/AGND set and be placed as close as possible to the power pins of DM9162. The conservative approach is to use two decoupling capacitors on each DVDD/DGND set and AVDD/AGND set. One 0.1μF is for low frequency noise, and the other 0.01μF is for high frequency noise on the power supply.
- The AVDD connection to the transmit center tap of the magnetic has to be well decoupled to minimize common mode noise injection from the power supply into the twisted pair cable. It is recommended that a 0.01μF decoupling capacitor should be placed between the center tap AVDD to AGND ground plane. This decoupling capacitor should be placed as close as possible to the center tap of the magnetic.10 uF or 47 uF Capacitor should be connected between each AVDD and AGND.

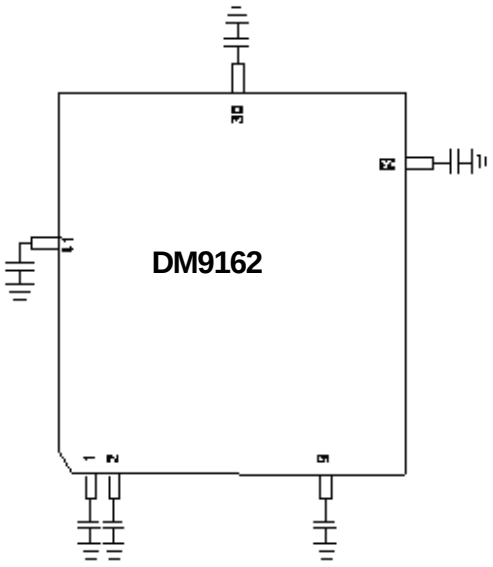


Figure 2

3. Ground Plane Layout

- Place a single ground plane approach to minimize EMI. Ground plane partitioning can cause increased EMI emissions that could make the network interface card (NIC) not comply with specific FCC part 15 and CE regulations.
- All AGND pins may not directly short each other (see Figure 3-3). It must be directly connected to analog ground domain (see Figure 3-2).

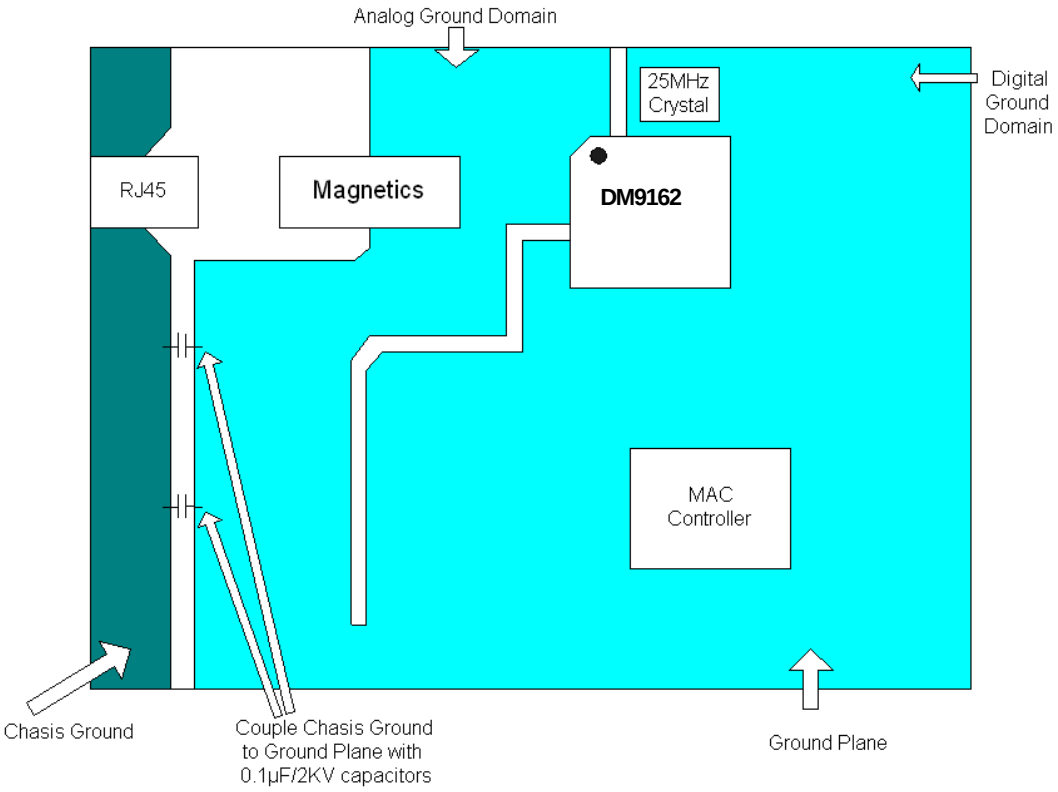


Figure 3-1

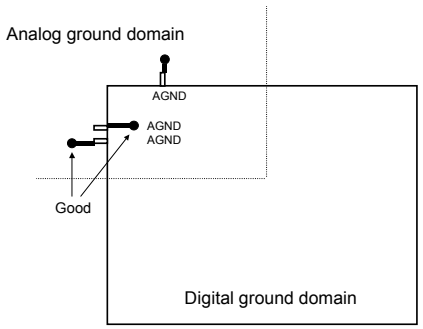


Figure 3-2

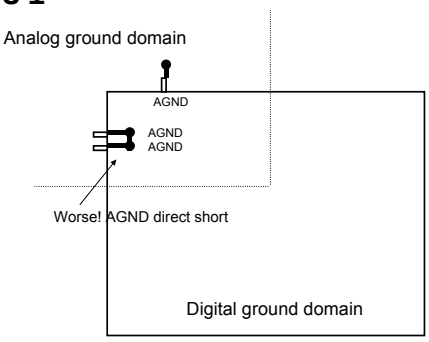


Figure 3-3

4. Power Plane Partitioning

- The power planes should be approximately illustrated in Figure 4. The ferrite bead used should have an impedance 100Ω at 100MHz and direct current rating of 400mA and above. A suitable bead is the Panasonic surface mound bead, part number EXCCL4532U or an equivalent. A 10μF, 0.1μF and 0.01μF electrolytic bypass capacitors should be connected between VDD and GND at the device side of each of the ferrite bead.
- Should separate analog power planes from noisy logic power planes.

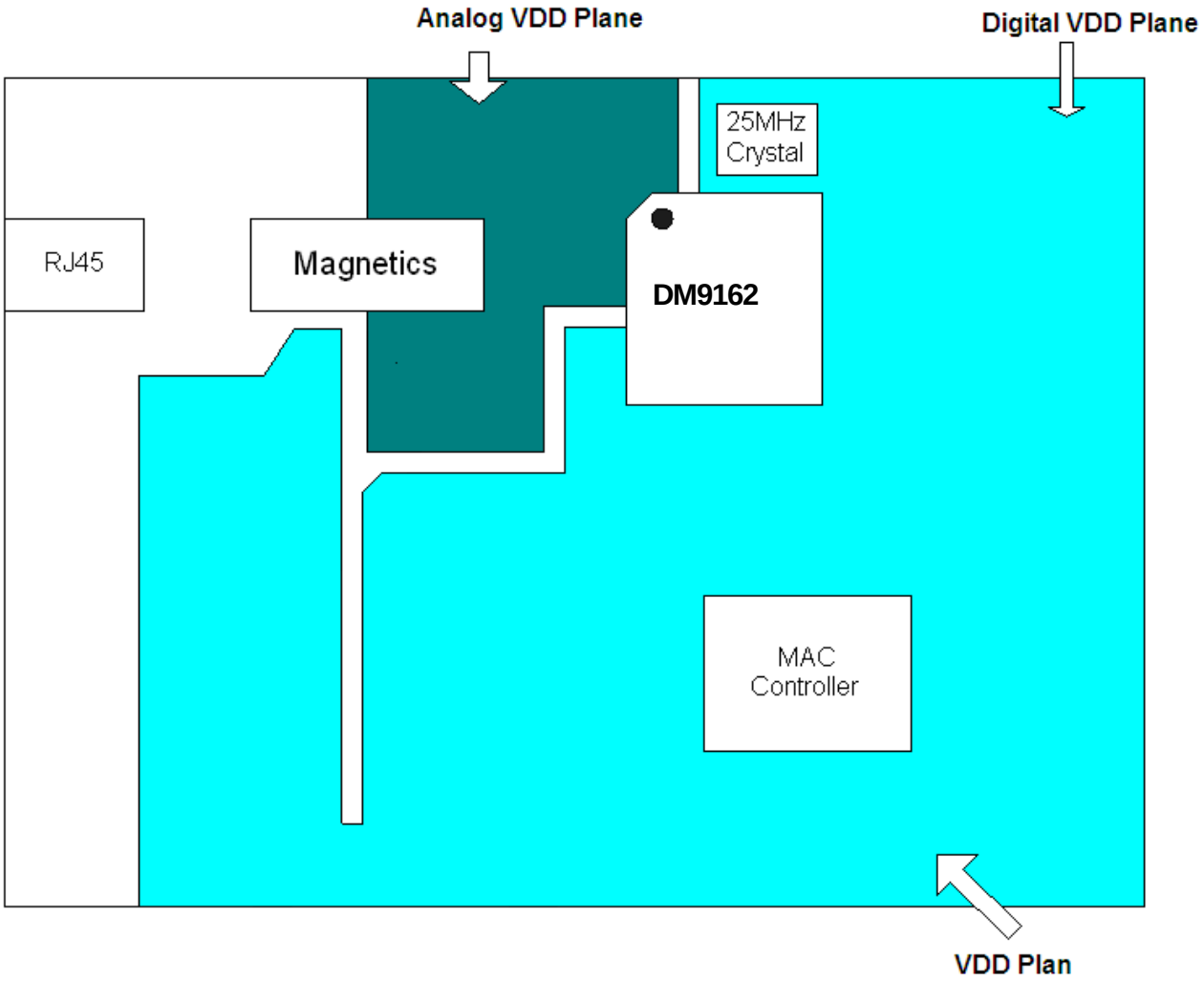


Figure 4

5. Magnetics Selection Guide

- Refer to the following tables 5-1 and 5-2 for 10/100M magnetic sources and specification requirements. The magnetics which meet these requirements are available from a variety of magnetic manufacturers. Designers should test and qualify all magnetic specifications before using them in an application. The magnetics listed in the following table are electrical equivalents, but may not be pin-to-pin equivalents.

Manufacturer	Part Number
MAGCOM`	HS9016, HS9024
Delta	LFE8563-DC, LFE8563T-DC

Table 5-1: 10/100M Magnetics Sources

Parameter	Values	Units	Test Condition
Tx / RX turns ratio	1:1 CT / 1:1	-	-
Inductance	350	μH (Min)	-
Insertion loss	1.1	dB (Max)	1 – 100 MHz
Return loss	-18	dB (Min)	1 –30 MHz
	-14	dB (Min)	30 – 60 MHz
	-12	dB (Min)	60 – 80 MHz
Differential to common mode rejection	-40	dB (Min)	1 – 60 MHz
	-30	dB (Min)	60 – 100 MHz
Transformer isolation	1500	V	-

Table 5-2: Magnetic Specification Requirements

6. Crystal Selection Guide

- A crystal can be used to generate the 25MHz reference clock instead of an oscillator. The crystal must be a fundamental type, series-resonant, connect to XT1 and XT2, and shunt each crystal lead to ground with a 22pF capacitor as shown in Figure 6.

PARAMETER	SPEC
Type	Fundamental, series-resonant
Frequency	25 MHz +/- 0.01%
Equivalent Series Resistance	25 ohms max
Load Capacitance	22 pF typ.
Case Capacitance	7 pF max.
Power Dissipation	1mW max.

Table 6-1: Crystal Specifications

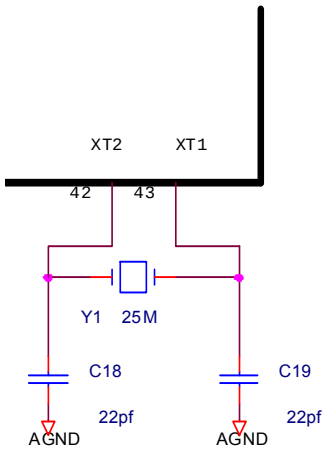


Figure 6
Crystal Circuit Diagram

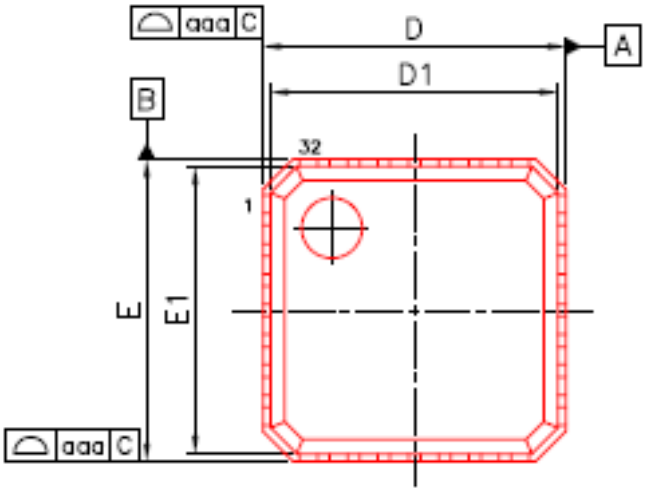
7. MII Signals to Mac Controller

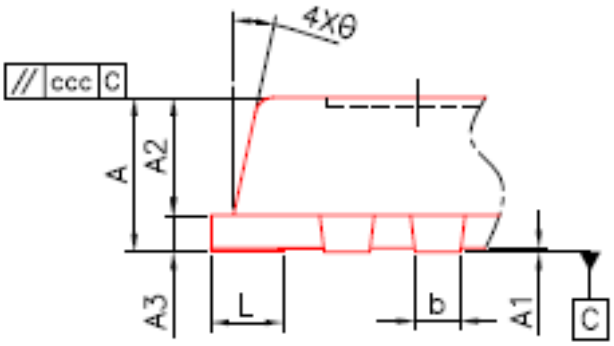
- The length of the trace routing for the Media Independent Interface (MII) signals should be as short and direct as possible between the DM9162 and MAC controller (Maximum length to be shorter than 20cm). These MII signals are as follows,

  CRS, COL, TXD3, TXD2, TXD1, TXD0, TXEN, TXCLK, TXER
  RXER, RXCLK, RXDV, RXD0, RXD1, RXD2, RXD3, MDC, MDIO

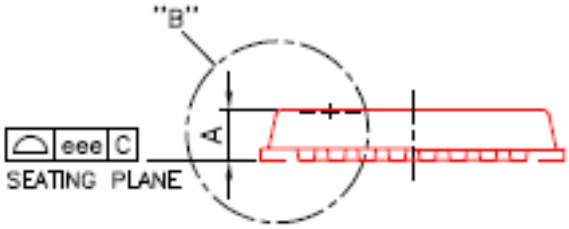
- TXD [0-3] and TXCLK length mismatch does not exceed 2cm.
- RXD [0-3] and RXCLK length mismatch does not exceed 2cm.
- All signal trace should be considered to have characteristic impedance of 50 Ohm.

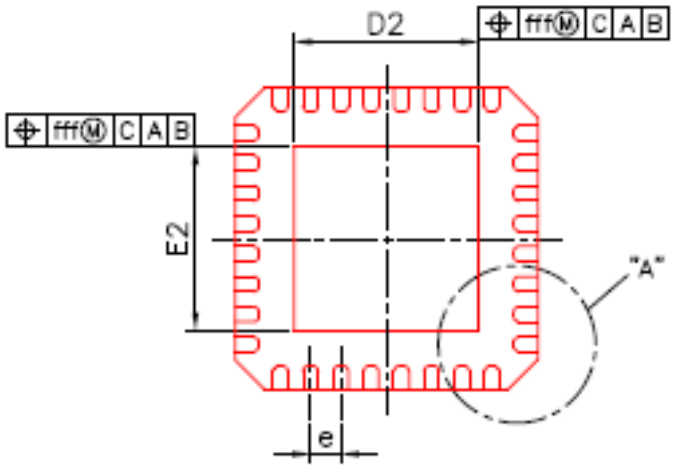
8. QFN Package PCB Layout note

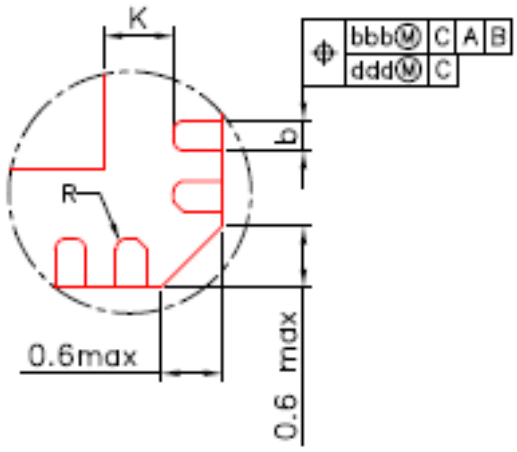




DETAIL : "B"







DETAIL : "A"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		5.00 BSC			0.197 BSC	
D1/E1		4.75 BSC			0.187 BSC	
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
ddd	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

Exposed Pad Size						
L/F	D2/E2 (mm)			D2/E2 (inch)		
	MIN	NOM	MAX	MIN	NOM	MAX
①	2.90	3.05	3.20	0.114	0.120	0.126
②	3.05	3.20	3.35	0.120	0.126	0.132
③	2.21	2.36	2.51	0.087	0.093	0.099
④	3.25	3.40	3.55	0.128	0.134	0.140
⑤	3.13	3.28	3.43	0.123	0.129	0.135
⑥	3.30	3.45	3.60	0.130	0.136	0.142

Exposed Pad size used is 3.4x3.4mm size.
The exposed pad is connected to ground plane for heat dissipation.
The ground connection between the component side and solder side of PCB for exposed pad area should be done with multiple vias. Each via having diameter of 0.3 mm and spaced evenly inside the exposed pad area with minimum spacing of 1 mm between them.

For assembly process, it is important to limit the amount of solder paste that is put under the exposed pad. If there are too much paste on the PCB, the package may float on top the paste during reflow process and misalign during soldering.
It is suggested for the solder mask to use a cross hatch pattern for the exposed pad area in order to reduce the amount solder paste put on the PCB.