DM9620A (RMII to USB)

Application Note

Version: V01

December 18, 2015

1. H/W Modification:

a. Pin42 pulled low with 4.7K

Pin No.	Pin Name	Description
42	TEST1	Test Mode 1 0: pins 11-13,15-16,18-22,24-27,33-34 as MII, RMII, Reverse MII interface

b. Strap pin setting

Pin No.	Pin Name	Description
12, 13	TXD3 TXD2	TXD3 TXD2 in external PHY mode 1 0 RMII
15	TXD1	0: EEPROM type auto-detection
16	TXD0	Ethernet RX packet header format 1= 4 header bytes include flag byte
30	EECS	0: 12MHz clock from internal PLL

1: pull-high 1K~10K, 0: default floating.

c. How to connect between CPU and DM9620A (Refer to Figure1)

RMII Interfaces

3.2 64-Pin LQFP Description

I = Input O = Output I/O = Input / Output

O/D = Open Drain P = Power PD = internal pull-low (about 50K Ohm)

3.2.2 RMII Interface

Pin No.	Pin Name	I/O	Description
26	MDC	O,PD	MII Serial Management Data Clock
27	MDIO	I/O	MII Serial Management Data
12,13	TXD3~2	O,PD	Reserved
15,16	TXD1~0	O,PD	RMII Transmit Data
11	TXE	O,PD	RMII Transmit Enable
18	TXC	I,PD	Reserved
33	CRS	I	Reserved, tie to ground in application.
34	COL	I	Reserved, tie to ground in application.
25	RXER	I	Reserved, tie to ground in application.
31	CLK50M	I	50MHz reference clock.
24	RXDV	I	RMII CRS_DV
19,20	RXD3~2	I	Reserved, tie to ground in application.
21,22	RXD1~0	I	RMII Receive Data

DM9620A(I) Reduce MII Block Diagram

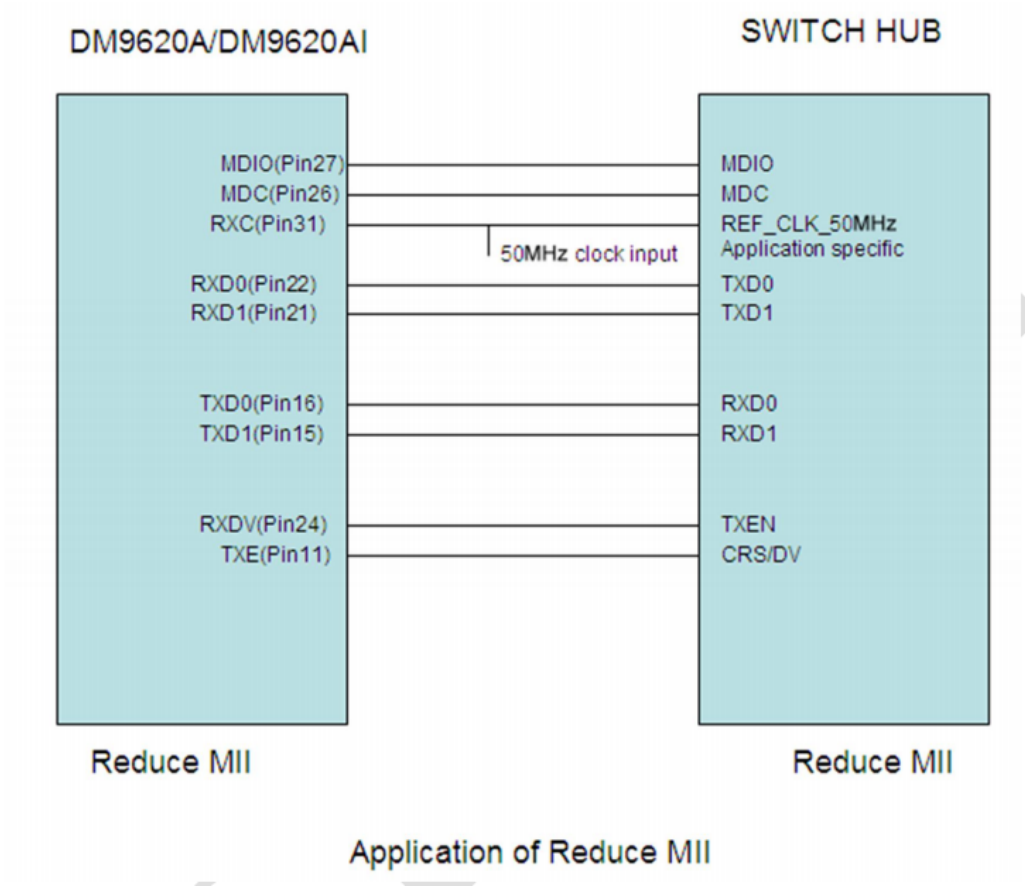

Figure 1

2. How to modify on DM9620A EVB

a. Remove R130 and Pull low TEST1 (pin42) with 4.7K as Figure2

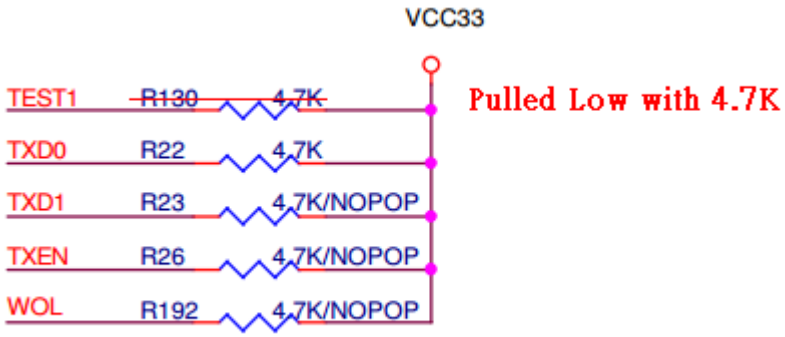

Figure 2

b. MII Interface

TXD3 (pin12) Pulled high with 4.7K for Reverse MII as Figure3.

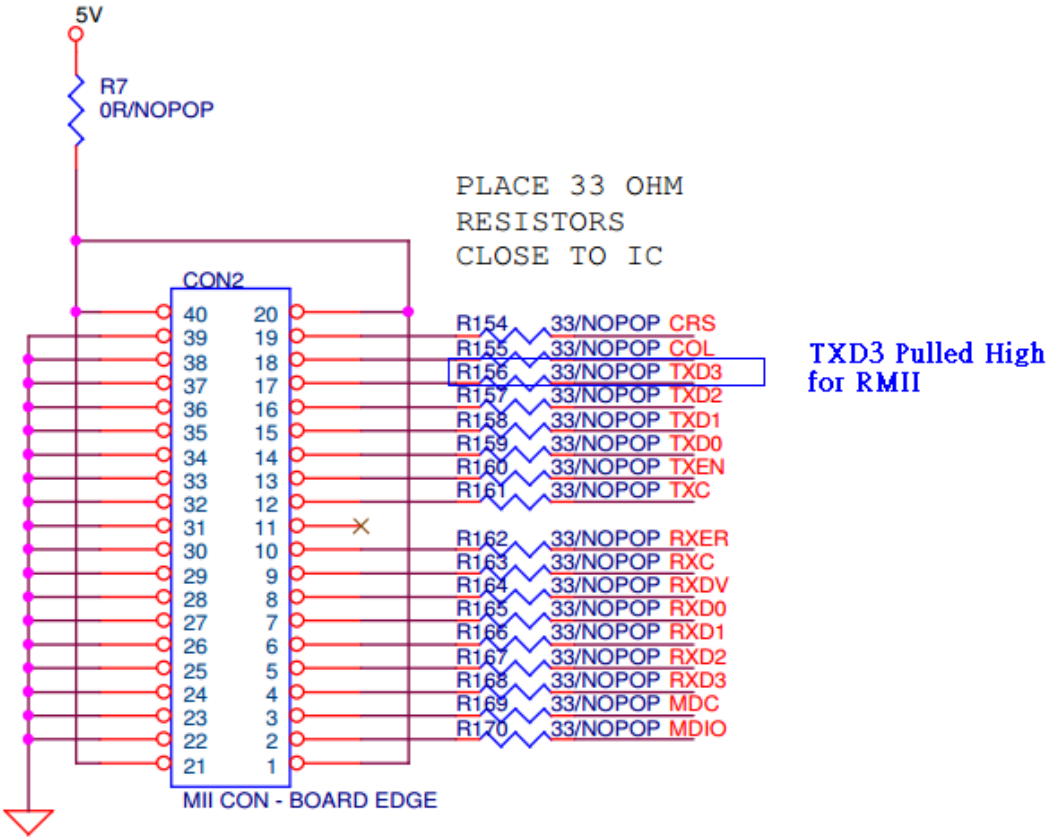

Figure3

c. Connected CON2 as Figure3 to CPU RMII with Figure1.

3. EEPROM

Use DM9620A (EXT MII) file from Davicom.

DM9620 (EXT MII) reference

Name	Word Offset	Value(Hex)
		9620A (Ext MII)
Auto Load Control	3	1551
Product ID	5	0268
802.3az control	6	008F
Wake-UP mode	7	4484
USB control	11	5A
EP3 interrupt interval	12[Low]	0010

String 2

DM9620A(Ext MII) String2 = "DM9620A USB To FastEther"

4. Driver

Use DM9620A Driver from Davicom.

Driver is identical and no need change when the H/W configure to be external MII/RMII/RevMII (TEST1 (pin42) tie to ground) and the connection is **100M Full Duplex** for the most cases.

(With the fewer case if connected MAC is 10M or Half Duplex, The register 2EH should be changed correspond to SPEED and/or DUPLEX bits. Keep LINK bit as 0 in order force to link ON in the application, Because no entity PHY exist in external PHY mode, the link state must be always link up state.)

a. After power on, EXT_PHY is 1 that is Select external PHY

4.1 Network Control Register (00H)

Bit	Name	Default	Description
7	EXT_PHY	PT0,RW	External PHY mode (valid when pin TEST1 tie to ground) 1: Select external PHY 0: select Internal PHY. This bit can be forced by register 2EH bit 5.

b. Also, EXTERNAL is 1 that is Force to external PHY mode, SPEED is 0 for 100Mbps mode, DUPLEX is 0 for full-duplex mode, LINK is 0 for link up state.

4.22 External PHY Force Mode Control Register (2EH)

Bit	Name	Default	Description
7:6	RESERVED	0,RO	Reserved
5	EXTERNAL	HP0,RW	Force to external PHY mode
4	RESERVED	0,RO	Reserved
3	RESERVED	PH0,RW	Reserved
2	SPEED	HP0,RW	Force external PHY speed mode in MAC register 1 bit 7 1: force to 10Mbps mode 0: force to 100Mbps mode
1	DUPLEX	HP0,RW	Force external PHY duplex mode in MAC register 0 bit 3 1: force to half-duplex 0: force to full-duplex
0	LINK	HP0,RW	Force external PHY link mode in MAC register 1 bit 6 1: force to link OFF 0: force to link ON

c. To add code to read/write phy registers (only when the MDC/MDIO is connect to the opposite chip which can provide MII registers read/write), ADR_EN must be 1, and EPHYADR[4:0] is the phy address. This can be the following example code, ‘phy’ is the phy address: dm_write_reg(dev, 0x33, 0x80 | phy);

4.25 External PHY Ceiver Address Register (33H)

Bit	Name	Default	Description
7	ADR_EN	HPS0,RW	**External PHY Address Enabled** When set in external MII mode, the external PHYceiver address is defined at bit 4:0.
6:5	Reserved	HPS0,RO	Reserved
4:0	EPHYADR	HPS01, RW	**External PHY Address Bit 4:0** The PHY address in external MII mode.