UZ2400

Silicon Version D

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

Registers Comparison Table

DS-2400-53

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UZ2400

Low Power 2.4 GHz Transceiver for IEEE 802.15.4 Standard

1. Introduction

This document describes the registers comparison between UZ2400 and UZ2400 Silicon Version D.

2. Modified Registers List

2.1. Short-Register

Offset	UZ2400		UZ2400 Silicon Version D	
	Register Name	Description	Register Name	Description
0x0D	RXFLUSH	Receive FIFO flush	RXFLUSH	Receive FIFO flush
0x26 GAT	ECLK	Gated clock control GA	TECLK	Gated clock control
0x29	HSYMTMR1	Half symbol timer[15:8]	HSYMTMR1	Half symbol timer[15:8]
0x30	RXSR	RX MAC status	RXSR	RX MAC status
0x33	GPIO	GPIO port	LASTRXSTA	RX MAC status of last frame
0x34	SPIGPIO	GPIO pin direction & SPI mode	PINGPONGRX	SPI mode & RX two FIFO mode
0x36	RFCTL	RF MODE control	RFCTL	RF MODE control
0x38	BBREG0	Baseband register 0	BBREG0	Baseband register 0

0x3A	BBREG2	Baseband register 2	BBREG2	Baseband register 2
0x3B	BBREG3	Baseband register 3	BBREG3	Baseband register 3
0x3C	BBREG4	Baseband register 4	BBREG4	Baseband register 4
0x3E	BBREG6	Baseband register 6	BBREG6	Baseband register 6

2.2. Long-Register

Offset	UZ2400		UZ2400 Silicon Version D	
	Register Name	Description	Register Name	Description
0x200	RFCTRL0	RF control register 0	RFCTRL0	RF control register 0
0x202	RFCTRL2	RF control register 2	RFCTRL2	RF control register 2
0x203	RFCTRL3	RF control register 3	RFCTRL3	RF control register 3
0x205	RFCTRL5	RF control register 5	RFCTRL5	RF control register 5
0x206	RFCTRL6	RF control register 6	RFCTRL6	RF control register 6
0x207	RFCTRL7	RF control register 7	RFCTRL7	RF control register 7
0x208	RFCTRL8	RF control register 8	RFCTRL8	RF control register 8

2.3. Short-Register description

Offset: 0x0D

	UZ2400				UZ2400 Silicon Version D			
	RXFLUSH				RXFLUSH			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**Reserved**				**RESERVED**			
6	**WAKEPOL**	Set polarity of WAKE signal: 0: Active low 1: Active high	0 R/W		**WAKEPOL**	Set polarity of WAKE signal: 0: Active low 1: Active high	1 R/	W
5	**WAKEPAD**	Turn on pad of the WAKE pin (pin 15).	0	R/W	**WAKEFPMB**	'0': means the external wakeup from pad mode is enable	1 R/	W
4	**reserved**				**RXFF_TEST**	Software can write any address of RXFIFO.	0 R/	W
3	**ONLYCMD**	Only command packet is allowed to receive.	0 R/W		**NM_NOCSMA**	Disable CSMA-CA for TX normal FIFO	0	R/W
2	**ONLYDATA**	Only data packet is allowed to receive.	0	R/W	**RESERVED**			
1	**ONLYBCN**	Only beacon packet is allowed to receive.	0 R/W					
0	**RXFLUSH**	Flush RXFIFO. This will not modify the data in RXFIFO but return pointers to zero. This bit is write to clear.	0 W	T	**RXFLUSH**	Flush RXFIFO. This will not alter data in RXFIFO, but return pointers to zero. This bit is automatically cleared.	0 W	T

Offset: 0x26

	UZ2400				UZ2400 Silicon Version D			
	GATECLK GATE				CLK			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**Reserved**				**TxB_ON**	Beacon FIFO clock always on	0	R/W
6					**TXN_OFF**	TXNFIFO clock always off	0	R/W
5					**SPI_SYNC**	Sync SPI interface – SEN and SCLK to prevent glitch Note: using this SPI is not functioning when main clock is turned off, meaning sleep mode.	0	R/W
4					**EN_RXM**	RXMAC clock always enable	0	R/W
3	**ENGTS**	Always enable GTS clock	0	R/W	**EN_GTS**	GTS clock always enable	0	R/W
2	**Reserved**				**EN_TRX**	TRX transaction clock always enable	0	R/W
1					**EN_SEC**	Security clock enable/disable when CTRL_SEC is '1'	0 R/	W
0					**CTRL_SEC**	Security clock controller	0	R/W

Offset: 0x29

	UZ2400				UZ2400 Silicon Version D			
	HSYMTMR1				HSYMTMR1			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-0	**HSYMTMR1**	High byte of 16-bit half-symbol timer	0	R/W	**HSYMTMR1**	Half symbol tick timer[15:8]. writing the register will start the timer	0 R/	W

Offset: 0x30

	UZ2400				UZ2400 Silicon Version D			
	RXSR				RXSR			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**Reserved**				**RXFFFull**	RX FIFO full	0	R
6	**UPSECERR**	MIC error in upper layer security mode	0	R/W1C	**WrFF1**	0: write data to RX FIFO 0 1: write data to RX FIFO 1	0 R	
5	**BATIND**	Battery low indicator	0	R	**UpperSecErr**	MIC error in upper layer security mode	0	R/W1C
4	**Reserved**				**RXFFOvfl**	RXFIFO overflow	0	R
3					**RXCrcErr**	RX CRC error flag, update when received each packet	0 R	
2					**SecDecErr**	Security decryption error	0	R
1					**RXHdrRdy**	RX Header ready	0	R
0					**PIDConflict**	PID conflict	0	R/W1C

Offset: 0x33

	UZ2400				UZ2400 Silicon Version D			
	GPIO				Last RX Status			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**Reserved**				**LRXFFFull**	RX FIFO full status of last frame	0	R
6					**LWrFF1**	0: write last frame to RX FIFO 0 1: write last frame to RX FIFO 1	0 R	
5	**GPIO5**	The status of GPIO5. Both read and write operations are allowed.	0 R/W		**Reserved**			
4	**GPIO4**	The status of GPIO4. Both read and write operations are allowed.	0 R/W		**LRXFFOvfl**	RXFIFO overflow status of last frame	0	R
3	**GPIO3**	The status of GPIO3. Both read and write operations are allowed.	0 R/W		**LRXCrcErr**	RX CRC error flag of last frame	0	R
2	**GPIO2**	The status of GPIO2. Both read and write operations are allowed.	0 R/W		**Reserved**			
1	**GPIO1**	The status of GPIO1. Both read and write operations are allowed.	0 R/W		**LRXHdrRdy**	RX Header ready status of last frame	0	R
0	**GPIO0**	The status of GPIO0. Both read and write operations are allowed.	0 R/W		**Reserved**			

Offset: 0x34

	UZ2400				UZ2400 Silicon Version D			
	SPIGPIO				SPI Mode & RX two FIFO			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-6	**SPIMODE**	Select the mode for SPI interface: 00: Normal SPI mode 01: PLUS SPI mode 10: Enhanced SPI mode	00 R	/W	**SPI_Mode**	SPI Mode: 00: normal 01: PLUS 10: TURBO	00 R	/W
5	**GPDIR5**	The direction of GPIO5: 0: Input direction 1: Output direction	0 R/W		BATIND	Battery low indicator	0 R	
4	**GPDIR4**	The direction of GPIO4: 0: Input direction 1: Output direction	0 R/W		**Reserved**			
3	**GPDIR3**	The direction of GPIO3: 0: Input direction 1: Output direction	0 R/W					
2	**GPDIR2**	The direction of GPIO2: 0: Input direction 1: Output direction	0 R/W		**WRFF1**	0: write data to RX FIFO 0 1: write data to RX FIFO 1	0 R	
1	**GPDIR1**	The direction of GPIO1: 0: Input direction 1: Output direction	0 R/W		**RdFF1**	0: read data from RX FIFO 0 1: read data from RX FIFO 1	0 R	
0	**GPDIR0**	The direction of GPIO0: 0: Input direction 1: Output direction	0 R/W		**RXFIFO2**	Indicator of RX FIFO which is selected to read. 0: read data from RX FIFO 0 1: read data from RX FIFO 1.	0 R	

Offset: 0x36

	UZ2400				UZ2400 Silicon Version D			
	RFCTL				RFCTL			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**Reserved**				**32m_en**	Enable 32MHz clock. When using external wake-up without SLPCLK, enable 32MHz by SW. It's automatically cleared.	0 W	
6					**Reserved**			
5					**Reserved**			
4-3	**WAKECNTEXT**	20MHz clock recovery time extension bits	0 R/W		**WakeCntExt**	Extension of WakeCnt in SReg35, total 16ms configurable.	0 R/	W
2	**RFRST**	RF state reset. Reset RF state. RF state must be reset in order to change the RF channels. Write "1" and then write "0" to accomplish the reset operation.	0 R/W		**RFRESET**	Set '1' to reset RF(turn off RF), set '0' to normal.	0 R/	W
1	**RFTXMODE**	RF is forced into TX mode	0	R/W	**RFTXMODE**	RF is forced to TX mode	0	R/W
0	**RFRXMODE**	RF is forced into RX mode	0	R/W	**RFRXMODE**	RF is forced to RX mode	0	R/W

Offset: 0x38

	UZ2400				UZ2400 Silicon Version D			
	BBREG0				BBREG0			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-4	**Reserved**				**preamble_cnt**	Number of preamble to send.	8	R/W
3					**Reserved**			
2					**Cont_tx**	Continuously send modulated random data	0 R/	W
1					**Sel_turbo**	00: Normal 250kbps 01: 1Mbps 11: 2Mbps 10: not available	0 R/	W
0	**TURBO**	Enable UZ2400 625kbps Turbo mode: 1: Turbo mode 0: Normal mode	0 R/W					

Offset: 0x3A

	UZ2400				UZ2400 Silicon Version D			
	BBREG2				BBREG2			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-6	**CCAMode**	CCA mode selection: 00: reserved 01: Carrier sense (CS) mode, detect IEEE 802.15.4 signals 10: Energy detection (ED) mode, detect in-band signals 11: Combination of carrier sense mode and energy detection mode	01 R	/W	CCAMODE	00: Reserved 01: CCA Mode 1 Ca rrier sense only 10: CCA Mode 2 Energy above threshold 11: CCA Mode 3 C arrier sense with energy above threshold	0x1 R	/W
5-2	**CCATH**	CCA carrier sense threshold NOTE: suggested value is 1110	0010 R/W		CCATH	CCA Carrier Sense Threshold Suggested Value: 0xE	0xf R	/W
1-0	**Reserved**				**Reserved**			

Offset: 0x3B

	UZ2400				UZ2400 Silicon Version D			
	BBREG3				BBREG3			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-4	**PREVALIDTH**	Baseband decoder parameter: 1101: normal mode (250kbps) optimized value 0011: turbo mode (625kbps) optimized value Do not use other values	1101	R/W	PREVALIDTH	Baseband decoder parameter 0b1101: is the optimized value for both normal and turbo modes.	0xd R	/W
3-1	**PREDETTH**	Baseband decoder parameter: 100 is the optimized value for both the normal and the turbo modes	100	R/W	PREDETTH	Baseband decoder parameter '0b1000' is the optimized value for both normal and turbo modes.	0x8 R	/W
0	**Reserved**							

Offset: 0x3E

	UZ2400				UZ2400 Silicon Version D			
	BBREG6				BBREG6			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**RSSIMODE1**	RSSI mode 1 enable: 1: calculate RSSI for firmware request, will be clear to "0" when RSSI calculation is finished	0x0 R	/W	**RSSI_Mode[1]**	RSSI mode 1 enable: 1: calculate RSSI for firmware request, will be clear to "0" when RSSI calculation is finished	0x0 WT	
6	**RSSIMODE2**	RSSI mode 2 enable: 1: calculate RSSI for each received packet, the RSSI value will be stored in RXFIFO 0: no RSSI calculation for received packet	0x0 R	/W	**RSSI_Mode[0]**	RSSI mode 2 enable: 1: calculate RSSI for each received packet, the RSSI value will be stored in RXFIFO 0: no RSSI calculation for received packet	0x0 R	/W
5	**Reserved**				**RSSI_max_latch**	For FW request mode, when this bit is set, LReg10 keeps the maximum RSSI value of several FW requests.	0x0 R	/W
4-1					**Reserved**			
0	**RSSIRDY**	RSSI ready signal for **RSSIMODE1** use: If **RSSIMODE1** is set, this bit will be cleared to "0" until RSSI calculation is done. When RSSI calculation is finished and the RSSI value is ready, this bit will be set to "1" automatically.	0x1 R		**Rssi_rdy**	RSSI ready signal for **RSSIMODE1** use: If **RSSIMODE1** is set, this bit will be cleared to "0" until RSSI calculation is done. When RSSI calculation is finished and the RSSI value is ready, this bit will be set to "1" automatically.	0x1 R	

2.4. Long-Register description

Offset: 0x200

	UZ2400				UZ2400 Silicon Version D			
	RFCTRL0				RFCTRL0			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-4	**CHANNEL**	IEEE 802.15.4 Channel Number 0000 : 2405 MHz Channel 11 0001 : 2410 MHz Channel 12 0010 : 2415 MHz Channel 13 0011 : 2420 MHz Channel 14 0100 : 2425 MHz Channel 15 0101 : 2430 MHz Channel 16 0110 : 2435 MHz Channel 17 0111 : 2440 MHz Channel 18 1000 : 2445 MHz Channel 19 1001 : 2450 MHz Channel 20 1010 : 2455 MHz Channel 21 1011 : 2460 MHz Channel 22 1100 : 2465 MHz Channel 23 1101 : 2470 MHz Channel 24 1110 : 2475 MHz Channel 25 1111 : 2480 MHz Chann el 26	0	R/W	**CH_N**	IEEE 802.15.4 Channel Number 0000 : 2405 MHz Channel 11 0001 : 2410 MHz Channel 12 0010 : 2415 MHz Channel 13 0011 : 2420 MHz Channel 14 0100 : 2425 MHz Channel 15 0101 : 2430 MHz Channel 16 0110 : 2435 MHz Channel 17 0111 : 2440 MHz Channel 18 1000 : 2445 MHz Channel 19 1001 : 2450 MHz Channel 20 1010 : 2455 MHz Channel 21 1011 : 2460 MHz Channel 22 1100 : 2465 MHz Channel 23 1101 : 2470 MHz Channel 24 1110 : 2475 MHz Channel 25 1111 : 2480 MHz Channel 26	0	R/W

3-0	**RFOPT**	Optimize RF performance: 0010 is the recommended value for RF optimization	0	R/W	**RFOPT**	Optimize RF performance: 0001 is the recommended value for RF optimization	0001	R/W

Offset: 0x202

	UZ2400				**UZ2400 Silicon Version D**			
	RFCTL2				RFCTRL2			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**PLLCTL**	RF Phase Lock Loop (PLL) control: 1: the recommended value for RF optimization.	0	R/W	**PLLCTL**	RF Phase Lock Loop (PLL) control: 1: the recommended value for RF optimization.	0	R/W
6-5	**RSSIDC**	RSSI DC level shift. Note: 11 is not allowed.	0 R	/W	**RFOPT**	Optimize RF performance: 11 is the recommended value for RF optimization.	00 R/W	
4-3	**RSSISLOPE**	RSSI range control. Note: 11 is not allowed.	00	R/W	**Reserved**	Please do NOT change default value	00	R/W

2-0	**Reserved**	Please do NOT change default value	000	R/W	ADC_REF	For adjusting RSSI reference level ADC reference level (mV) 000: 625; 001: 650; 010: 675; 011: 700; 100: 725; 101: 750; 110: 775;111: do not use (forbidden) 110 is the recommended value for RF optimization	0x0 R	/W

Offset: 0x203

	UZ2400				UZ2400 Silicon Version D			
	RFCTL3				RFCTRL3			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-6	**TXPOWL**	Large scale control for TX power in dB: 00: 0 dB 01: -10 dB 10: -20 dB 11: -30 dB	00 R/W		TXG_B	TX back e nd s tepped g ain c ontrol (nominal value in dB) 00000: 0 dB; ..... 11111: -8 dB	000 R	/W
5-3	**TXPOWF**	Fine scale control for TX power in dB: 000: 0 dB 001: -0.5 dB 010: -1.2 dB 011: -1.9 dB 100: -2.8 dB 101: -3.7 dB 110: -4.9 dB 111: -6.3 dB	000	R/W				
2-0	**Reserved**	Please do NOT change default value	000	R/W	**Reserved**	Please do NOT change default value	000	R/W

Offset: 0x204

	UZ2400				UZ2400 Silicon Version D			
	RFCTL4				RFCTRL4			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-0	**Reserved**	Please do NOT change default value	0	R/W	**Reserved**	00000011 is the recommended value for RF optimization	0000	R/W

Offset: 0x205

	UZ2400				UZ2400 Silicon Version D			
	RFCTL5				RFCTRL5			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-4	**BATTH**	Battery monitor threshold value corresponding to voltage supply: 1110 : 3.5V 11 01 : 3.3V 1100 : 3.2V 10 11 : 3.1V 1010 : 2.8V 10 01 : 2.7V 1000 : 2.6V 01 11 : 2.5V Other : out of operation voltage	0000	R/W	**BAT_TH**	Battery Low Voltage Detection Threshold (V) 0000 : 1.8V 00 01 : 1.9V 0 010 : 2.0V 0011 : 2.1V 01 00 : 2.2V 0 101 : 2.3V 0110 : 2.4V 01 11 : 2.5V 1 000 : 2.6V 1001 : 2.7V 10 10 : 2.8V 1 011 : 2.9V 1100 : 3.0V 11 01 : 3.2V 1 110 : 3.4V 1111 : 3.6V	0000	R/W
3-0	**Reserved**	Please do NOT change default value	0000	R/W	**Reserved**	Please do NOT change default value	0000	R/W

Offset: 0x206

	UZ2400				UZ2400 Silicon Version D			
	RFCTL6				RFCTRL6			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7	**TXFIL**	TX filter control: 1: the recommended value for RF optimization.	0 R	/W	TX_BW	TX filter bandwidth control 00: 2.5 MHz ; 01: 5 MHz; 10: 7.5 MHz ; 11: 10 MHz 00 is the recommended value for RF optimization	11 R/W	
6	**Reserved**	Please do NOT change default value	0	R/W				
5-4	**20MRECVR**	20MHz clock recovery time (recovery from sleep) control: 10: less than 1 ms Otherwise: less than 3ms	0	R/W	32MClk_boost	Current mode of 32MHz crystal driver 00 : 100 uA ; 01 : 300 uA ; 10 : 400 uA ; 11 : 600 uA 11 is the recommended value for RF optimization	11 R/W	
3	**BATEN**	Battery monitor enable: 1: Battery monitor is enabled 0: Battery monitor is disabled	0 R	/W	**BATon**	Battery monitor on or off: 0: off; 1: on	0 R	/W
2-0	**Reserved**	Please do NOT change default value	000	R/W	**Reserved**	Please do NOT change default value	000 R	/W

Offset: 0x207

	UZ2400				UZ2400 Silicon Version D			
	RFCTL7				RFCTRL7			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-6	**SLPCLK**	Sleep clock source selection: 10: internal ring oscillator 01: external crystal 10: internal ring oscillator	0	R/W	**ClkOutMode**	Output Clock Frequency 000 : 1 MHz ; 001 : 2 MHz ; 010 : 4 MHz ; 011 : 8 MHz ; 100 : 16 MHz ; 101 : 32 MHz ; 110 : 32 MHz ; 111 : OFF 111 is th e recommended value for saving current consumption	000	R/W
5	**Reserved**	Please do NOT change default value	0	R/W				
4	**Reserved**	Please do NOT change default value	0	R/W	**RX_LPF**	RX lowpass filter on or off 0: on; 1: off	0	R/W
3-2	**Reserved**	Please do NOT change default value	00	R/W	**Reserved**	Please do NOT change default value	00	R/W
1-0	**CLKDIV**	UZ2400 output clock frequency selection: 00: 2.5MHz 01: 5MHz 10: 10MHz 11: 20MHz Note: If the external 32.768kHz crystal is not connected, SLPCLK needs to be set to 10.	00	R/W	**Reserved**	Please do NOT change default value	00	R/W

Offset: 0x208

	UZ2400				UZ2400 Silicon Version D			
	RFCTL8				RFCTRL8			
Bits	**Name**	**Description**	**Reset Value**	**R/W**	**Name**	**Description**	**Reset Value**	**R/W**
7-6	**Reserved**	Please do NOT change default value	00	R/W	**Div2_Boost**	Div-by-2 Current Option for TX Mode 00 : 1 mA ; 01 : 1.2 mA ; 10 : 1.6 mA ; 11 : 1.8 mA	00	R/W
5	**Reserved**	Please do NOT change default value	0	R/W	**LO_Boost**	LO Buffer Current Option 00 : 2.0 mA ; 01 : 2.4 mA ; 10 : 2.8 mA ; 11 : 3.2 mA	00	R/W
4	**RFVCO**	VCO control. Recommend value is "1"	0 R	/W				
3-2	**Reserved**	Please do NOT change default value	0	R/W	**Reserved**	Please do NOT change default value	0	R/W
1	**Reserved**	Please do NOT change default value	0	R/W	**Fast_VCO_Cal**	Fast VCO Calibration Mode Control 0 : Disable ; 1 : Enable	0 R	/W
0	**CLKOUTSRC**	The source of 20MHz clock output: 0: From analog module. Unstable when recovering from sleep mode. 1: From power management module. Stable when recoverin from sleep mode.	0 R	/W	**Reserved**	Please do NOT change default value	0	R/W

3. Additional Long Registers of UZ2400 Silicon Version D

3.1. Long-Register

Offset	Register Name	Description
0x3c	RX_FRM_TYPE	Frame Type of RX packet filtering
0x3d GP	IO_DIR	GPIO direction
0x3e GPIO		GPIO ports
0x4d SEC	_APP	Security appended functions
0x4e	ENC_FLG	Encryption flag in initial block
0x4f	AUT_FLG	Authentication flag in initial block
0x50	RFCTRL50	RF control register 50
0x51	RFCTRL51	RF control register 51
0x52	RFCTRL52	RF control register 52
0x53	RFCTRL53	RF control register 53
0x54	RFCTRL54	RF control register 54
0x55	RFCTRL55	RF control register 55
0x59	RFCTRL59	RF control register 59
0x5e	RFCTRL5E	RF control register 5E
0x73	RFCTRL73	RF control register 73
0x74	RFCTRL74	RF control register 74

0x75	RFCTRL75	RF control register 75
0x76	RFCTRL76	RF control register 76
0x7a	INIT_CTR0	Security counter low byte in initial block
0x7b	INIT_CTR1	Security counter high byte in initial block

3.2. Long-Register description

LREG3C: RXFRMTYPE

Offset: 0x23C

Bits	Name	Description	Reset Value	R/W
7-0	**RXFRMTYPE**	RX packet filter. Packet type field in 'Frame control" byte of IEEE802.15.4 is 3 bits, meaning 8 types of packets.Each bit of RXFRM_TYPE correlated to the 8 types. When correlated bit is '1', RXMAC receives the type of packet without filtering it out. RXFRM_TYPE[0] : 000 (beacon) RXFRM_TYPE[1] : 001 (data) RXFRM_TYPE[2] : 010 (ack) RXFRM_TYPE[3] : 011 (command) RXFRM_TYPE[4] : 100 (Reserved) RXFRM_TYPE[5] : 101 (Reserved) RXFRM_TYPE[6] : 110 (Reserved) RXFRM_TYPE[7] : 111 (Reserved)	0x0b R/W	

LREG3D: GPIODIR

Offset: 0x23D

Bits	Name	Description	Reset Value	R/W
7-6	**Reserved**			
5	**GPDIR5**	GPIO 5 direction, '0': output '1': input	1	R/W
4	**GPDIR4**	GPIO 4 direction '0': output '1': input	1	R/W
3	**GPDIR3**	GPIO 3 direction '0': output '1': input	1	R/W
2	**GPDIR2**	GPIO 2 direction '0': output '1': input	1	R/W
1	**GPDIR1**	GPIO 1 direction '0': output '1': input	1	R/W
0	**GPDIR0**	GPIO 0 direction '0': output '1': input	1	R/W

LREG3E: GPIO

Offset: 0x23D

Bits	Name	Description	Reset Value	R/W
7-6	**Reserved**			
5	**GPIO5**	GPIO5	0	R/W
4	**GPIO4**	GPIO4	0	R/W
3	**GPIO3**	GPIO3 status	0 R	/W
2	**GPIO2**	GPIO2 status	0 R	/W
1	**GPIO1**	GPIO1 status	0 R	/W
0	**GPIO0**	GPIO0 status	0 R	/W

LREG4D: SEC_APP

Offset: 0x4d

Bits	Name	Description	Reset Value	R/W
7	**Reserved**			
6	**AES_ONLY**	Trigger AES only mode SW should set it '0' to come back. Trigger when '0' to '1'.	0x0 R	/W
5	**SEC_2006**	Change CTR mode in IEEE802.15.4-2003 to ENC mode in IEEE802.15.4-2006	0x0	R/W
4	**USR_FLG_CTR**	Use user-defined 'flag' and 'initial counter'. User-defined flag: LReg4E, LReg4F User-defined counter: LReg7A, LReg7B	0x0 R	/W
3-1	**Reserved**			

0	**AES_ONLY_RDY**	AES only mode complete. Setting AES_ONLY bit clears the status. Report '1' when complete AES process.	0x0 R	

LREG4E: ENC_FLG

Offset: 0x24E

Bits	Name	Description	Reset Value	R/W
7-0	**ENC_FLG**	The initial flag is used for encryption in CCM/CCM* mode. In 802.15.4-2003, the flag is set automatically to: CTR: 0x82 OTHER: 0x01 In other cases, setting ENC_FLG can define customized value.	0x0 R/W	

LREG4F: AUT_FLG

Offset: 0x24F

Bits	Name	Description	Reset Value	R/W
7-0	**AUT_FLG**	The initial flag is used for authentication for CBC-MAC mode. In 802.15.4-2003, the flag is set automatically to correlated flags with different MIC lengths. In other cases, setting AUT_FLG can define the customized value.	0x0 R	/W

LREG0x250: RFCTRL50

Bits	Name	Description	Reset Value	R/W
7-5	Reserved	Please do NOT change default value	0	R/W
4	DCDC_ON	DC/DC Converter Power ON Control 0 : Bypass 1 : Enable	0 R	/W

3-0	Reserved	Please do NOT change default value	0	R/W

LREG0x251: RFCTRL51

Bits	Name	Description	Reset Value	R/W
7-4	Reserved	Please do NOT change default value	0	R/W
3-2 L	atch_time	Lock Detector Latch Time 00 : 46u sec ; 01 : 46.4u sec ; 10 : 52.8u sec ; 11 : 59.2u sec	0x0 R	/W
1 LOCK_r	es	Lock Detector Reset 0: Reset ; 1: Start Count Lock (Rising edge)	0 R	/W
0 L	OCK_en	Lock Detector Enable 0: Disable 1: Enable	0	R/W

Note: The initial register value set by software : 0x251=0xc0

**Lock Detector Testing Proceture : LLREG0x251[1:0]= 01 → 11 → 01 → Read LREG0x25e

LREG0x252: RFCTRL52

Bits	Name	Description	Reset Value	R/W
7-1	Reserved	Please do NOT change default value	0x00	R/W
0 32	MHz_Xtal_Startup	Start-Up Circuit of 32MHz Crystal Oscillator Control 0: Disable; 1: Enable;	1 R	/W

Note: The initial register value set by software : 0x252=0x01

LREG0x253: RFCTRL53

Bits	Name	Description	Reset Value	R/W
7	Reserved	Please do NOT change default value	0	R/W
6 FI	FO	FIFO Power in Sleep Mode 0 : VDD_Wake 1 : GND	0 R	/W
5 D	igital	Digital Power in Sleep Mode 0 : VDD_Wake 1 : GND	0 R	/W
4 Standby		32MHz Crystal Oscillator Standby Mode Control 0: Disable 1: Enable	0 R	/W
3	PA3_90uA_ En<0>	PA Control 1 Enable:1 ; D isable:0	0	R/W
2-0	PA3_90uA <2:0>	PA current fine tune 001: 20uA; 001: 40uA ; 010: 60uA ; 011: 80uA ; 100: 120uA ; 101: 140uA; 110: 160uA ; 111: 180uA	0x0	R/W

Note: The initial register value set by software : 0x253=0x00 (For 0dBm TX output power setting)

LREG0x254:RFCTRL54

Bits	Name	Description	Reset Value	R/W
7 1M	Hz_EN	1MHz Resolution Channel Control 1 : Enable (1MHz channel spacing) ; 0 : IEEE 802.15.4 channel (5MHz channel spacing)	0 R	/W
6-0	1MHz_Freq_Table	Channel Table Mapping (**)	0x00	R/W

** Channel Table Mapping:

0000000 : 2400 MHz	0010000 : 2416 MHz	0100000 : 2432 MHz	0110000 : 2448 MHz	1000000 : 2464 MHz
0000001 : 2401 MHz	0010001 : 2417 MHz	0100001 : 2433 MHz	0110001 : 2449 MHz	1000001 : 2465 MHz
0000010 : 2402 MHz	0010010 : 2418 MHz	0100010 : 2434 MHz	0110010 : 2450 MHz	1000010 : 2466 MHz
0000011 : 2403 MHz	0010011 : 2419 MHz	0100011 : 2435 MHz	0110011 : 2451 MHz	1000011 : 2467 MHz
0000100 : 2404 MHz	0010100 : 2420 MHz	0100100 : 2436 MHz	0110100 : 2452 MHz	1000100 : 2468 MHz
0000101 : 2405 MHz	0010101 : 2421 MHz	0100101 : 2437 MHz	0110101 : 2453 MHz	1000101 : 2469 MHz
0000110 : 2406 MHz	0010110 : 2422 MHz	0100110 : 2438 MHz	0110110 : 2454 MHz	1000110 : 2470 MHz
0000111 : 2407 MHz	0010111 : 2423 MHz	0100111 : 2439 MHz	0110111 : 2455 MHz	1000111 : 2471 MHz
0001000 : 2408 MHz	0011000 : 2424 MHz	0101000 : 2440 MHz	0111000 : 2456 MHz	1001000 : 2472 MHz
0001001 : 2409 MHz	0011001 : 2425 MHz	0101001 : 2441 MHz	0111001 : 2457 MHz	1001001 : 2473 MHz
0001010 : 2410 MHz	0011010 : 2426 MHz	0101010 : 2442 MHz	0111010 : 2458 MHz	1001010 : 2474 MHz
0001011 : 2411 MHz	0011011 : 2427 MHz	0101011 : 2443 MHz	0111011 : 2459 MHz	1001011 : 2475 MHz
0001100 : 2412 MHz	0011100 : 2428 MHz	0101100 : 2444 MHz	0111100 : 2460 MHz	1001100 : 2476 MHz
0001101 : 2413 MHz	0011101 : 2429 MHz	0101101 : 2445 MHz	0111101 : 2461 MHz	1001101 : 2477 MHz
0001110 : 2414 MHz	0011110 : 2430 MHz	0101110 : 2446 MHz	0111110 : 2462 MHz	1001110 : 2478 MHz
0001111 : 2415 MHz	0011111 : 2431 MHz	0101111 : 2447 MHz	0111111 : 2463 MHz	1001111 : 2479 MHz

1010000 : 2480 MHz	1010100 : 2484 MHz	1011000 : 2488 MHz	1011100 : 2492 MHz	The Rest : 2495 MHz
1010001 : 2481 MHz	1010101 : 2485 MHz	1011001 : 2489 MHz	1011101 : 2493 MHz	
1010010 : 2482 MHz	1010110 : 2486 MHz	1011010 : 2490 MHz	1011110 : 2494 MHz	
1010011 : 2483 MHz	1010111 : 2487 MHz	1011011 : 2491 MHz	1011111 : 2495 MHz	

Note: The initial register value set by software: 0x254=0x00

LREG0x255: RFCTRL55

Bits	Name	Description	Reset Value	R/W
7-6	Reserved	Please do NOT change default value	0x0	R/W
5 H	alt	Halt Mode Control 0 : Halt Mode Diable 1 : Halt Mode Enable **Note : Before entering Halt Mode, LREG0x277=0x04 needs to be set.**	0	R/W
4-0	Reserved	Please do NOT change default value	0x00	R/W

Note: The initial register value set by software : 0x255=0x00

LREG0x259: RFCTRL59

Bits	Name	Description	Reset Value	R/W
7-1	Reserved	Please do NOT change default value	0x00	R/W
0 Si	gma-Delta	Fractional Spur Control 0 : Not Remove Fractional Spur 1 : Remove Fractional Spur	0 R	/W

Note: The initial register value set by software : 0x259=0x00

LREG0x25e : RF Status 0:

Bits	Name	Description	Reset Value	R/W
7-2 R	eserved			
1 Loc	k_out_i	Lock Detector Indicator ● Lock_ready_i = 0 Lock Detector is NOT ready ● Lock_ready_i = 1 Lock_out_i = 0 : PLL Lock Lock_out_i = 1 : PLL Unlock	0	R

LREG0x273: RFCTRL73

Bits	Name	Description	Reset Value	R/W
7-6 V	CO_C	VCO Current Level for TX Mode 00 : 4.5X ; 0 1 : 4X 10 : 3.5X ; 1 1 : 2.5X	00 R	/W
5-0	Reserved	Please do NOT change default value	0	R/W

Note: The initial register value set by software : 0x273=0x80

LREG0x274: RFCTRL74

Bits	Name	Description	Reset Value	R/W
7	PA1_900uA_ En<0>	PA Control 1 Enable:1 ; Disable:0	1 R	/W
6-4	PA1_900uA <2:0>	PA current rough tune 000: 150uA; 001: 300uA ; 010 : 450 uA ; 011: 600 uA ; 100 : 900 uA ; 101: 1050 uA ; 110: 1200 uA ; 111: 1350 uA;	100 R	/W
3	PA2_180uA_ En<0>	PA Control 2 Enable:1 ; Disable:0	1 R	/W
2-0	PA2_180uA <2:0>	PA voltage control for output stage 001: 15uA; 001: 30uA ; 010: 45uA ; 011: 60uA ; 100: 90uA ; 101: 105uA; 110: 120uA ; 111: 135uA	010 R	/W

Note: The initial register value set by software : 0x253=0xc4 (For 0dBm TX output power setting with DC/DC ON), 0x253=0xc6 (For 0dBm TX output power setting with DC/DC OFF)

LREG0x275: RFCTRL75

Bits	Name	Description	Reset Value	R/W
7-5	Reserved	Please do NOT change default value	0	R/W
4	Slow_Clock_ Select	Slow Clock Selection 0: 32 KHz Crystal Oscillator 1: Integrated Ring Oscillator	**1**	R/W

3	Reserved	Please do NOT change default value	0	R/W
2-0	Slow_Clock_ Current	32 KHz Crystal Oscillator Current Option 000: 0.8 uA; ..... 111: 6.2 uA Ring Oscillator Current Option 000: 0.5 uA; ..... 111: 2.8 uA	0101 R/W	

Note: The initial register value set by software : 0x275=0x13 (For Integrated Ring Oscillator)

LREG0x276: RFCTRL76

Bits	Name	Description	Reset Value	R/W
7-5	Reserved	Please do NOT change default value	0x0	R/W
2 B	uffer_SW	Slow Clock Buffer Switch Control 0 : OFF ; 1 : ON	0	R/W
1-0	Ring_Osc _Current	Ring Osc Current Option 00 : Smallest Current ; ..... 11 : Largest Current	1	R/W

Note: The initial register value set by software : 0x276=0x07

LREG0x277: RFCTRL77

Bits	Name	Description	Reset Value	R/W
7-6	**Reserved**	Do NOT change the default value	0x0	R/W
5-4	**Sleep_Mode_Control**	Sleep Mode Control 00 : Standby mode 01 : Deep sleep mode 10 : Forbidden 11 : Power down mode	0x0 R	/W
3	**VDD_Wake_Control**	VDD_Wake Voltage Control 1 : Automatically controlled by internal circuit ; 0 : Controlled by LREG0x277<1:0>	1 R	/W
2	**Reserved**	Do NOT change the default value	0	R/W
1-0	**VDD_Wake_Voltage**	VDD_Wake Voltage Selection 00 : Highest Voltage ; ..... 11 : Lowest Voltage	0x0 R	/W

Note: The initial register value set by software : 0x277=0x08

LREG7A: INIT_CTR0

Offset: 0x27A

Bits	Name	Description	Reset Value	R/W
7-0	**INIT_CTR0**	When AES_ONLY, SEL_2006 or UPPER_CIPHER modes, if USR_FLG_CTR is set to '1', {INIT_CTR1, INIT_CTR0} will replace the counter bytes of the initial encryption block.	0x0 R/W	

LREG7B: INIT_CTR1

Offset: 0x27B

Bits	Name	Description	Reset Value	R/W
7-0	**INIT_CTR1**	When AES_ONLY, SEL_2006 or UPPER_CIPHER modes, if USR_FLG_CTR is set to '1', {INIT_CTR1, INIT_CTR0} will replace the counter bytes of the initial encryption block.	0x0 R/W	

Revision History

Revision	Date	Description of Change
1.0 2	009/05/04	Original

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